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Issue 6/2008

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THE 2008 DSP DIRECTORY

PEEL AWAY THE LAYERS OF COMPLEXITY

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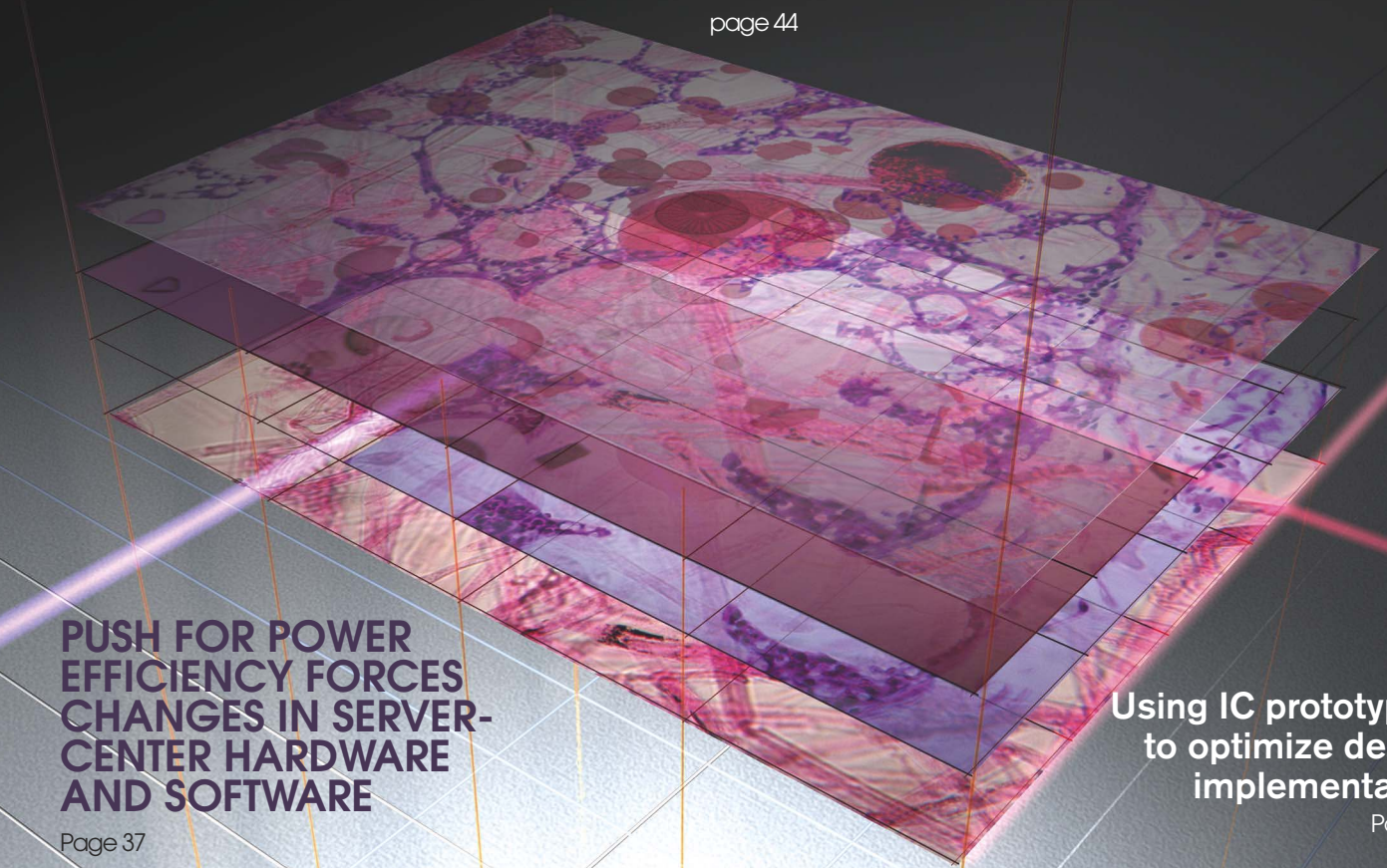

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DIGITAL TV FOR THE FUTURE: hybrid analog/ digital-TV-receiver design

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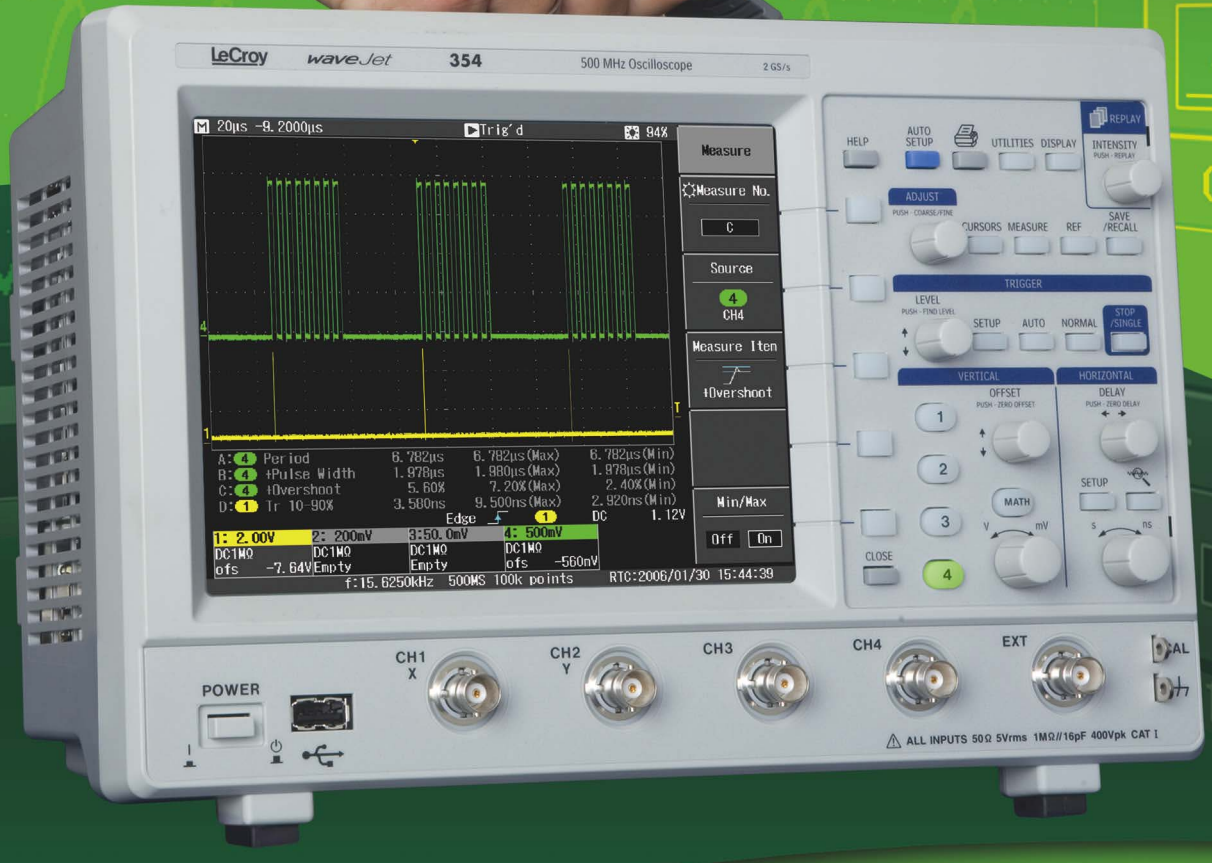

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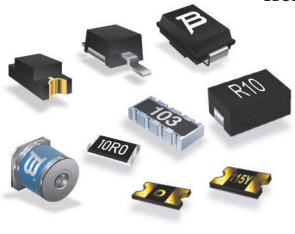

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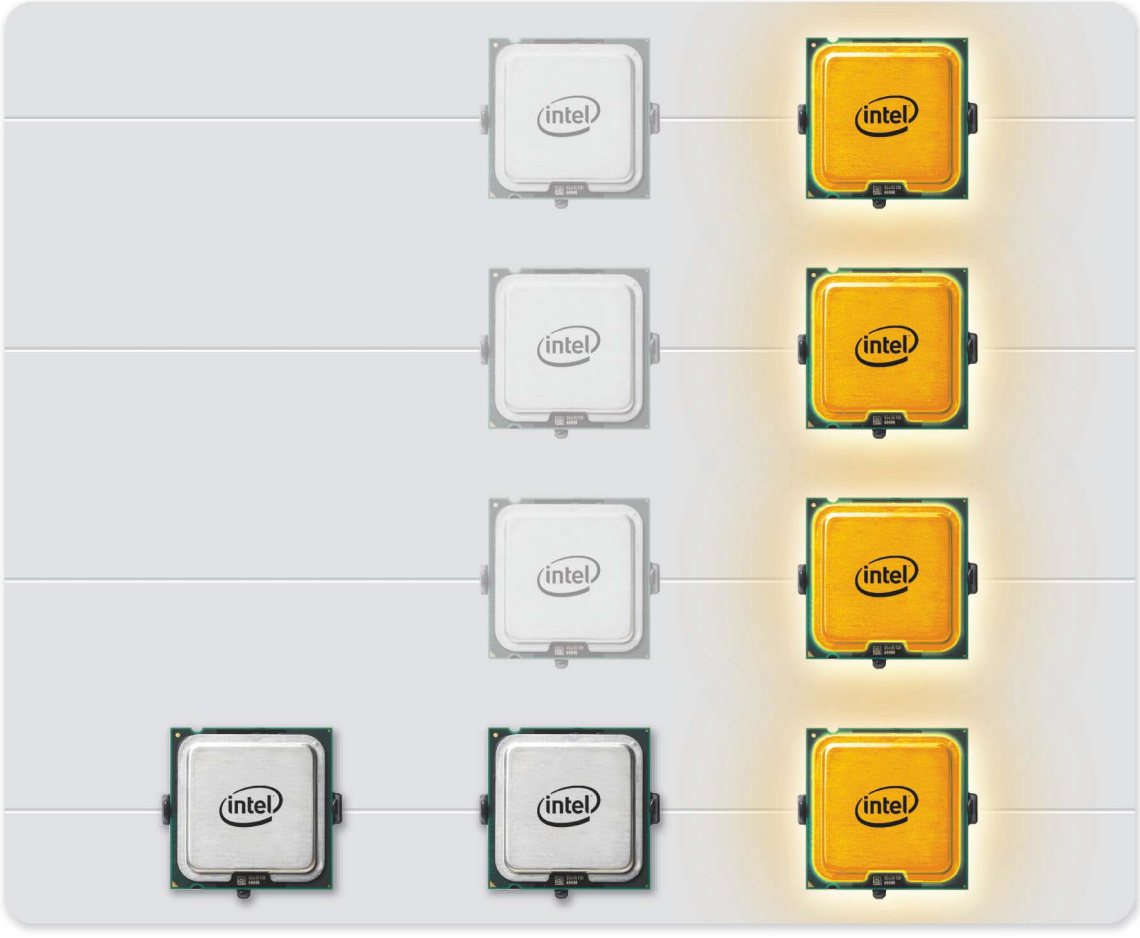

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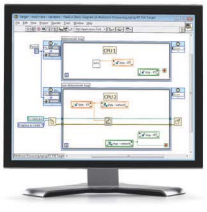

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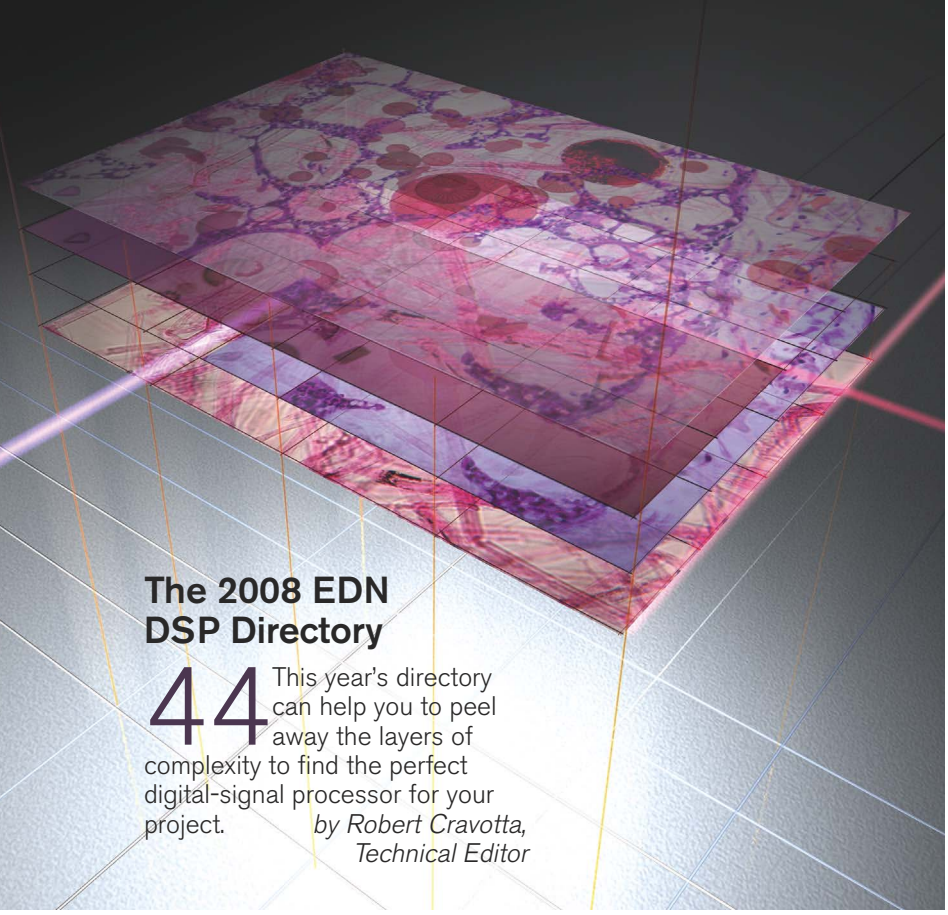

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3.20.08

The 2008 EDN DSP Directory

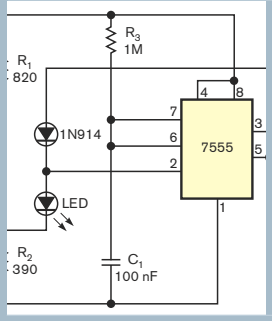
Push for power efficiency forces changes in server-center hardware and software

Using IC prototyping to optimize design implementation

Trip points for IC-timing analysis

Digital TV for the future: hybrid analog/digital-TV-receiver design

DESIGNIDEAS



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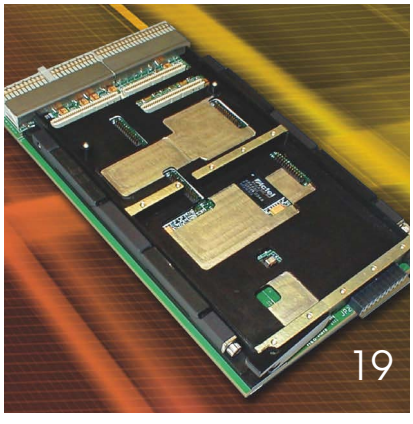

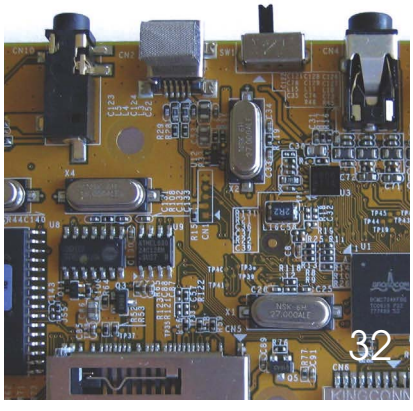

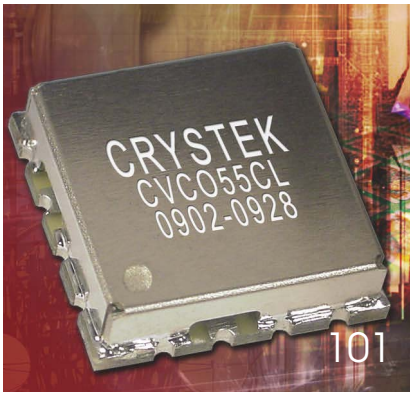

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EDN® (ISSN#0012-7515), (GST#123397457) is published biweekly, 26 times per year, by Reed Business Information, 8878 Barrons Blvd, Highlands Ranch, CO 80129-2345. Reed Business Information, a division of Reed Elsevier Inc, is located at 360 Park Avenue South, New York, NY 10010. Tad Smith, Chief Executive Officer; Mark Finkelstein, President, Boston Division. Periodicals postage paid at Littleton, CO 80126 and additional mailing offices. Circulation records are maintained at Reed Business Information, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. Telephone (303) 470-4445. POSTMASTER: Send address changes to EDN®, PO Box 7500, Highlands Ranch, CO 80163-7500.

Rates for nonqualified subscriptions, including all issues: US, $165 one year; Canada, $226 one year, (includes 7% GST, GST#123397457); Mexico, $215 one year; air expedited, $398 one year. Except for special issues where price changes are indicated, single copies are available for $10 US and $15 foreign. Publications Agreement No. 40685520. Return undeliverable Canadian addresses to: RCS International, Box 697 STN A, Windsor Ontario N9A 6N4. E-mail: Subsmail@ReedBusiness.com. Please address all subscription mail to EDN®, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. EDN® is a registered trademark of Reed Elsevier Properties Inc, used under license. A Reed Business Information Publication/Volume 53, Number 6 (Printed in USA).

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designideas

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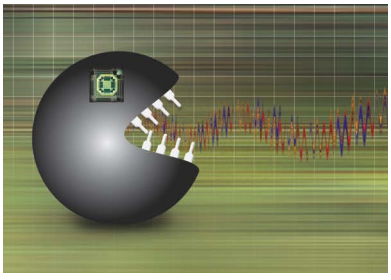


READER'S CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

As SOCs grow, test-and-measurement instruments move on-chip
Complex ICs are not only absorbing more of the systems around them, but also swallowing the test equipment designers use to bring up, evaluate, and calibrate the chips.
→www.edn.com/article/CA6531583

Siemens cuts 3800 jobs, plans plant sales
Siemens AG lays out a restructuring plan that calls for some 3,800 job cuts as it moves its Siemens Enterprise Communications subsidiary from being a hardware supplier to a software provider in the harsh telecommunications market.
→www.edn.com/article/CA6535492

Delta-sigma ADCs in a nutshell, part 3: the digital/decimator filter
A digital-filter function attenuates the noise, and the decimator function slows the output-data rate.
→www.edn.com/article/CA6531581

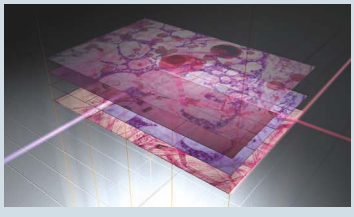
NE555 timer sparks low-cost voltage-to-frequency converter
The combination of an NE555 timer and a Miller integrator yields a voltage-to-frequency converter that costs less than 50 cents.
→www.edn.com/article/CA6531584

Optoisolators compute watts and volt-amperes
Relying on the dynamic conductance of optoisolators' junctions, simple optoisolator bridges compute the watts and volt-amperes of an ac load.
→www.edn.com/article/CA6531585

FROM *EDN*'S BLOGS

Thermal versus magnetic circuit breakers
From Anablog, by Paul Rako
Because of an experience when I worked for GMC Truck and Coach 30 years ago, I have always thought that thermal circuit breakers were not very good. Yet, a recent experience with a thermal breaker seems to prove they work fine when you properly design and specify them.
→www.edn.com/080320toc1

Staying on the Accelerating Technology Treadmill
From Brian's Brain, by Brian Dipert
You might wonder why I'm holding onto any of my 802.11 adapters, given the commonality of integrated Wi-Fi nowadays. The short answer is that commonality doesn't yet equate to ubiquity. There are plenty of places in my home, for example, where running Category 5 cable would be a hassle and power-line networking might be sketchy….
→www.edn.com/080320toc2



DSP-directory gold mine
Technical Editor Robert Cravotta's DSP directory is chock-full of hidden treasure. It includes **tables** that allow you to do side-by-side product comparisons and select just the right device for your project. It also includes information that expands greatly on the print edition. Do some mining of your own; you may find the mother lode.
→www.edn/dspdirectory.com.

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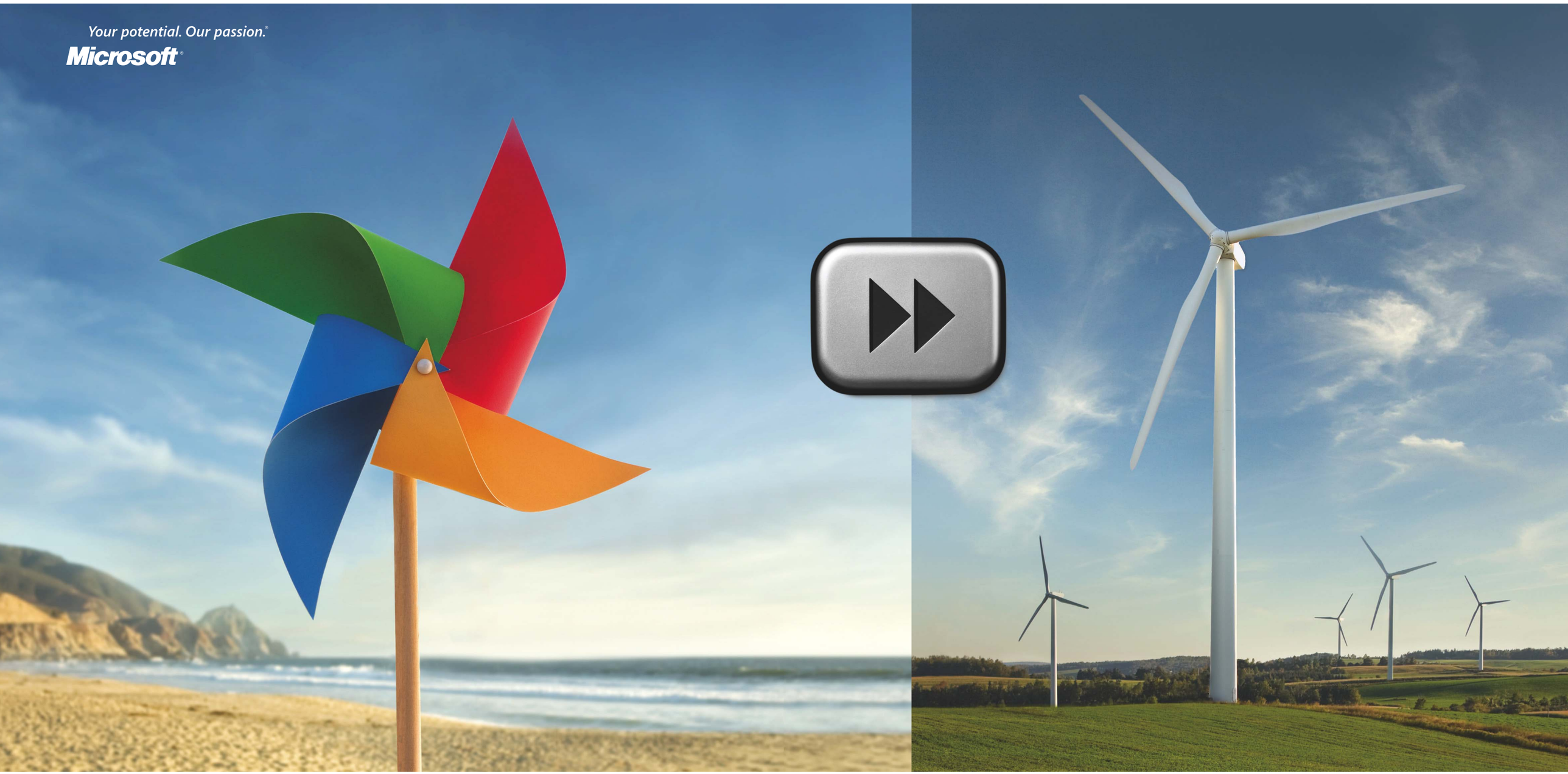

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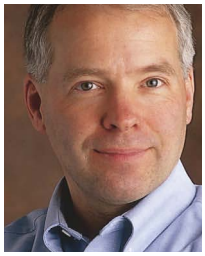

BY RICK NELSON, EDITOR-IN-CHIEF

External instruments here to stay

I recently commented on embedded instruments, noting that software that inserts testability structures into designs and that helps analyze test results to improve yield will become increasingly important as traditional instruments lose access to circuit nodes buried within deep-submicron ICs, multichip packages, and BGA-populated PCBs (printed-circuit boards). (See "Embedded instruments," *Test & Measurement World*, December 2007/January 2008, pg 7 www.tmworld.com/article/CA6514353).

Then, *EDN* Executive Editor Ron Wilson addressed the topic from a chip-centric point of view (see "As SOCs grow, test-and-measurement instruments move on-chip," *EDN*, Feb 21, 2008, pg 31, www.edn.com/article/CA6531583). In addition to citing lack of test-probe access, he notes that "As critical circuits reach gigahertz frequencies, it becomes physically impossible to get an accurate representation of signals off the die, even if you can probe the circuit." Nevertheless, he continues, manufacturing engineers must be able to develop low-cost test strategies, and designers must be able to create autocalibration routines that can compensate critical circuits for process, voltage, temperature, impedance, and noise variations while the chip is in use." He adds that "The only apparent option is to move the test-and-measurement instruments … onto the chip itself."

Companies pursuing embedded-instrument strategies include DAFCA, Cisco, ARM, Analog Devices, Rambus, STMicroelectronics, Vitesse, and ASE. Wilson details the technologies of several of these companies in his article. The methods by which embedded instruments communicate with the outside world, however, are just as important as the internal details of embedded-instrument technology.

Verigy's purchase of Inovys speaks to the importance of the external hardware/software combination in testing today's state-of-the-art chips.

Al Crouch, chief scientist at Inovys, now part of Verigy, addressed the migration of instruments into chips in an International Test Conference presentation last fall titled "The Need for Standard and Efficient Interconnection and Access of Embedded-Everything." In that talk, he noted that embedded instruments can serve in system-level test as well as chip-level test. A chip might work fine when you plug it into a $10,000 load board that connects to a $2 million ATE (automated-test-equipment) system, he said, but added that, when you pack it onto a 5×5-in. board with 10 other chips and connect it to a $35 power supply, it might turn out not to work so well—an issue that embedded-system-level test can address effectively.

Crouch also commented that the proliferation of embedded instruments presents its own problems involving the need to effectively communicate with them. He concluded that the IEEE P1687 internal JTAG initiative can provide an effective way for orderly, standardized embedded-instrument communication and control.

Whatever the interface standard, real external instruments and systems that gather test data and external software that performs yield-learning and other analysis tasks must supplant embedded instruments. Verigy's purchase of Inovys speaks to the importance of the external hardware/software combination in testing today's state-of-the-art chips.

Certainly, chip-test equipment is migrating from multimillion-dollar "big-iron" systems to something more cost-effective. The industry and media will address the pace of this evolution throughout the year. For instance, I'll be moderating a panel on this and other topics at the Third Annual GSC (Global Semiconductor Test Consortium) Conference, convening June 4 through 6 in San Diego, in partnership with the Design Automation Conference, convening the following week in Anaheim, CA. But whatever form the evolution takes, it would be a mistake to assume that embedded instruments will make external instruments go away. EDN

Contact me at rnelson@reedbusiness.com.

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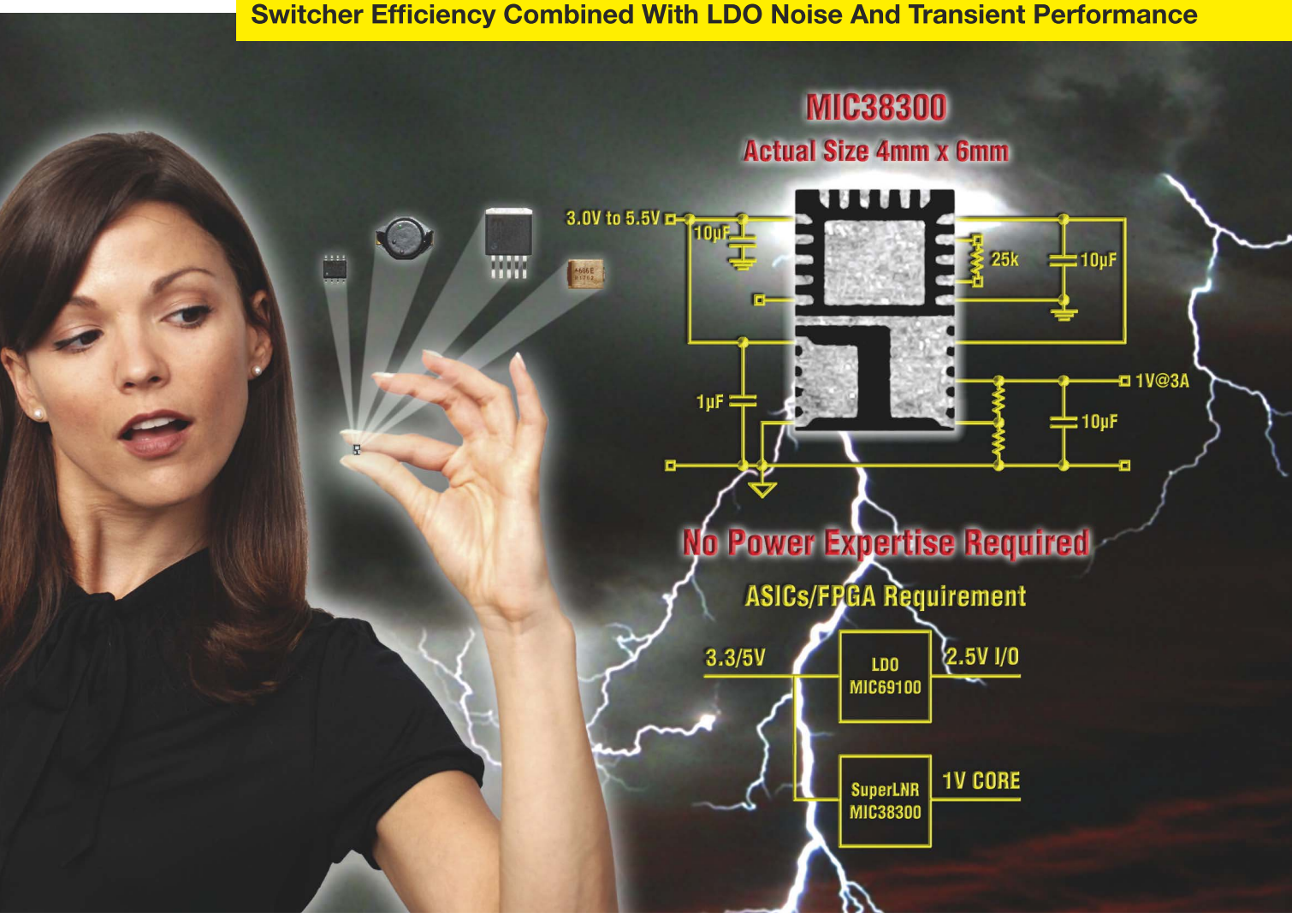

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Muna Acosta, Applications Engineer

As early as 1950, electro-chemical sensors were used for oxygen (gas) monitoring; however, with increasing concerns about personal safety, the demand for portable electro-chemical sensors has dramatically increased. Today, electro-chemical sensors are commonly used in portable equipment to detect different toxic gases.

Electro-chemical sensors operate by reacting with monitored gas and producing an electrical current that is linearly proportional to the gas concentration. Older versions of electro-chemical sensors were based on a two-electrode configuration; however, to achieve superior electro-chemical stability, three-electrode systems are now used. The three electrodes are stacked parallel to each other, separated by a thin layer of electrolyte that provides ionic electrical contact between the electrodes.

Sensor Functionality

When a gas comes in contact with the sensor, it passes through a thin membrane barrier to reach the electrode surface. The first electrode that the gas comes in contact with is the Working Electrode (WE). The WE is designed to optimize the electro-chemical oxidation, (or reduction of the measured gas), and to generate a current flow that is proportional to the gas concentration.

The performance of the sensor deteriorates over time due to the continuous electro-chemical reaction of the changes in WE potential occurring on the electrode. To reduce deterioration while maintaining a constant sensitivity with a good linearity, a Reference Electrode (RE) is placed close to the WE. The reference electrode's purpose is to anchor the working electrode at the correct potential. In order for the RE to maintain a constant potential, no current should flow through it.

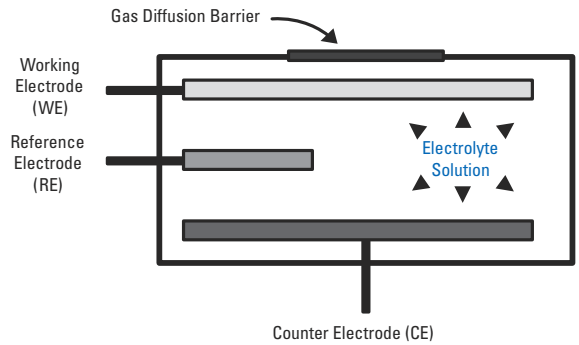

Figure 1. Typical Electro-chemical Sensor

The third electrode, the Counter Electrode (CE), conducts current into or out of the sensor cell. When the WE oxidizes carbon monoxide, the counter electrode reduces other molecules, such as oxygen to generate current. This current exactly balances the current generated at the WE. The ionic current between the working electrodes and counter is transported by the electrolyte.

Potentiostatic Circuit Operation

Electro-chemical sensors require control circuitry to operate. The control circuitry is referred to as the Potentiostatic Circuit. ***Figure 2*** shows a simplified potentiostatic circuit which is comprised of two amplifiers and one JFET transistor. There are small variations in the implementation of this circuit, but the function and the outcome are the same.

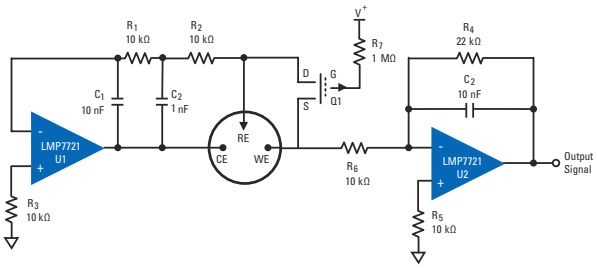

Figure 2. Potentiostatic Circuit

The potentiostatic circuit's main purpose is to maintain a voltage between the reference electrode and the working electrode to control the electro-chemical reaction and to deliver an output signal proportional to the WE current.

When the sensor is exposed to the target gas, such as carbon monoxide, the reaction at the WE oxidizes the carbon monoxide to become carbon dioxide, which diffuses out of the sensor. Hydrogen ions and electrons are generated. The hydrogen ions migrate through the electrolyte towards the counter electrode. This process leaves a negative charge deposited on the working electrode. The electrons flow out from the working electrode through resistor R6 to the inverting input of the amplifier (U2). The amplifier

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is configured as a transimpedance amplifier, which will convert the signal current from the WE into a voltage proportional to the applied gas concentration.

Output Voltage = I_{sensor} (R4+ R6)/R4

For example, a 10 ppm carbon monoxide sample produces a typical signal current of approximately 500 nA, which will give an output voltage of 5 mV. The hydrogen ions that have migrated toward the counter electrode will lift the potential of the RE and the WE. This small rise in potential at the RE is measured by the control amplifier (U1). The amplifier will sink or source adequate current to the CE to balance the current required by the working electrode.

The P-type JFET is used as a switch to prevent the sensor from polarizing when the circuit has no power. If the sensor is polarized, it will take the sensor a long time to stabilize at equilibrium. The JFET is only active when the power is off and at this time it shorts the WE and RE to ensure that the working electrode is maintained at the same potential as the reference electrode.

Amplifier Selection is Critical

The performance of the potentiostatic circuit is greatly dependent on the electrical parameters of the amplifiers chosen. Designing a potentiostatic circuit using a high-bias current amplifier without precision specifications will impact the sensor sensitivity and increase sensor to sensor variation. A precision, ultra-low input bias current amplifier, such as National's LMP7721, improves the potentiostatic circuit's performance, which allows the electro-chemical sensor to detect low-gas concentration with high accuracy.

The LMP7721 is designed with input bias guard driver circuitry to dramatically reduce the input bias current over the common mode voltage range to a typical of 3 fA at room temperature. Guaranteed specifications of 20 fA at room temperature and 900 fA at 85°C makes the LMP7721 the lowest temperature guaranteed bias current amplifier available.

In the potentiostatic circuit, the input bias current of the control amplifier (U1) is one of the critical specifications. The inverting input of U1 which is connected to RE, can-

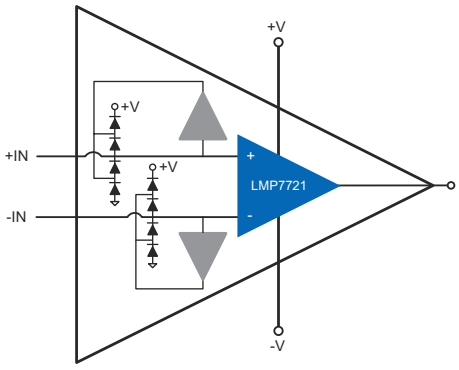

Figure 1. Typical Electro-chemical Sensor

not draw any significant current from the reference electrode. The LMP7721 ultra-low input bias amplifier will assure that the reference electrode will maintain constant potential by having less then 3 fA of bias current.

In addition, gas sensors have large capacitance, so significant currents can flow for small potential shifts; therefore, the offset voltage and offset drift over temperature are critical. A precision amplifier such as the LMP7721 with a maximum input offset voltage of 180 µV, and temperature drift of 4 µV/°C will enable more accurate current measurements. An amplifier with larger offset adds to the bias voltage of the sensor's working electrode causing more error.

In conclusion, the majority of gas sensors are three-electrode electro-chemical cells that generate current that is linearly proportional to the gas concentration. The generated current is measured and converted to a voltage by the potentiostatic circuit. The potentiostatic circuit also provides the current to the counter electrode to balance the current required by the working electrode. The electrical specifications of the amplifiers used in the circuit should be precision with ultra-low bias current, such as National's LMP7721 amplifier.

For more information, visit:
national.com/analogedge

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EDITED BY FRAN GRANVILLE

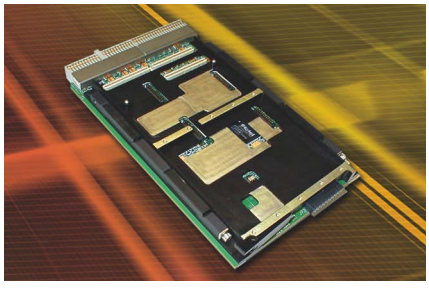
pulse

INNOVATIONS & INNOVATORS

Customizable CPU platform combines DSP, FPGA

Critical Link recently announced the MityDSP-Pro customizable processing platform, which targets data- and processing-intensive applications, including embedded radar control and signal processing, high-data-rate real-time data acquisition, image processing, and fine-tolerance manufacturing test. The standard module integrates a 1.2-GHz Texas Instruments (www.ti.com) TMS320C6455 DSP with a Xilinx (www.xilinx.com) XC3S2000 Spartan 3 FPGA, flash-memory and DDR2 SDRAM subsystems, and support for four one-lane serial-RapidIO links. Both the DSP and the FPGA can load and execute programs and logic images that end users develop.

"The MityDSP-platform approach enables a project to begin with 80% of the work complete by using an off-the-shelf CPU module and existing interface designs," says Tom Catalino, the company's vice president. These elements quickly provide the combination for a custom application without the cost or scheduling problems of ground-up design, he says. The platform supports analog-to-digital, digital-to-analog, Ethernet, and general-purpose-I/O interfaces. The MityDSP-Pro standard-version module sells for $1295 (100).



The MityDSP-Pro reconfigurable-CPU platform collects, processes, and delivers data at processor speeds as high as 1.2 GHz.

—by Warren Webb

▷**Critical Link, LLC,** www.criticallink.com.

FEEDBACK LOOP

"Only an analog engineer could be so down to earth!"

—Reader Madhav Dhaneshwar, commenting on Technical Editor Paul Rako's article about overengineering. Read more and add your own comments in *EDN*'s Feedback Loop, at www.edn.com/article/CA6518684.

DSP with hardware acceleration transcodes HD in real time

Texas Instruments recently unveiled the TMS320DM6467 chip, the latest in the company's DaVinci DSP line. The chip targets use in real-time-video transcoding; it handles high-definition video. The chip has an ARM core for control processing—in this case, a 926EJ-S—and a 600-MHz C64x+ DSP core. This variant includes a video coprocessor into which TI hard-coded transcoding-HD video, a conversion engine, and appropriate video-interface ports.

It performs simultaneous multiformat HD encoding, decoding, and transcoding of 1080p at 30 frames/sec or 1080i/720 at 60 frames/sec. The coprocessor and hardware acceleration deliver power equivalent to 3 GHz in a programmable DSP; offloading the main DSP engine in this way leaves more than half of its processing capability available for application code.

The conversion engine also hosts hardware chroma sampling and handles overlay of menus. Target markets are media gateways, video telephony, and video security, in which the system handles multiple channels of standard-definition video. In this scenario, the set-top box becomes tomorrow's "digital-media adapter," routing video to and from any format, from big-screen HD to cell-phone displays.

The processing load that this chip handles would previously have required three 6415T DSPs, with more associated RAM and fl ash memory and a larger FPGA. The new part sells for $35.95 (50,000). TI supports it with its standard tool chain, accessing third-party software intellectual property; an evaluation module runs MontaVista Linux.

—by Graham Prophet

▷**Texas Instruments**, www.ti.com.

Popularly priced scopes' display-update rates outpace competition

Agilent Technologies has expanded its MSO (mixed-signal-oscilloscope)- and DSO (digital-storage oscilloscope)-product lines with 10 models in the next-generation InfiniiVision 7000 Series. The units deliver what the company calls an unparalleled deep-memory display-update rate of 100,000 waveforms/sec. The new series offers bandwidths as high as 1 GHz, analog-signal-sampling rates as high as 4G samples/sec on each active channel, and memory depths as great as 8M points/channel with half of the analog channels and none of the MSOs' digital channels active. All models are in 7-in.-deep packages that weigh 14 lbs and feature the industry's largest displays—12.1-in. XGA (1024×768-pixel) LCDs whose area is more than 35% greater than those of competitive scopes.

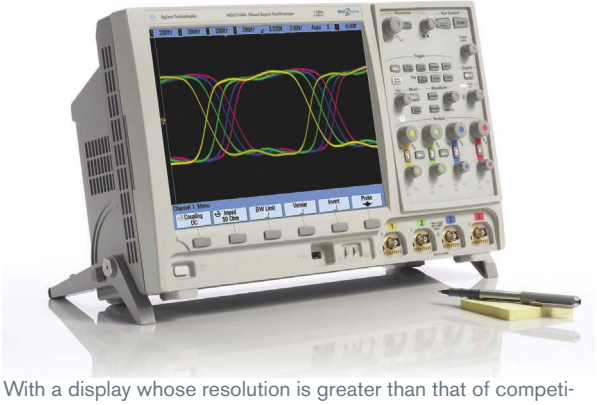
To appreciate how much faster the 7000 Series units update their displays than do competitive instruments, you need to perform a side-by side comparison, and you may initially wonder why Agilent makes such a big deal of display-update rate. But if you wait a few minutes and closely observe the displays, you should be impressed. In a demo at *EDN*'s offices, a glitch appeared on the 7000 Series MSO display after about 3 seconds, whereas it took a competitive MSO more than five minutes to display an identical glitch in the same signal. In fact, the glitches occurred periodically at a low duty cycle, but, if you wait a predetermined interval for the glitch to appear on screen, the smaller the fraction of the time the scope is "blind," the higher its probability of displaying such a glitch. "Blind time" refers to periods when a scope processes data it has already acquired and can't acquire new data. In the 7000 Series, Agilent has dramatically reduced blind time and has thus correspondingly increased the percentage of time during which the scope can acquire new data.

The math says that we might occasionally have had to wait for more than two hours for the competitive scope to display the glitch. Joel Woodward, the Agilent senior product manager who conducted the demo, says that measurements he made at his office confirmed his two-hour prediction. His point, though, was that if we hadn't known that the glitch existed, it was highly unlikely that we would we have waited long enough to notice it. Yet, finding infrequently occurring glitches that you don't know exist is a key function of scopes used for troubleshooting. Because they spend so much more of their time on signal acquisition, the 7000 Series scopes dramatically reduce the time required to find glitches, metastable states, and other elusive phenomena. And, because few engineers will wait for hours while nothing seems to be happening, the 7000s can reveal problems that competitive units simply miss.

Agilent also boasts that the 7000 Series offers the industry's most comprehensive suite of applications, including serial decoding and triggering for I^2C (inter-IC), SPI (serial-peripheral-interface), CAN (controller-area-network), LIN (local-interconnect-network), and FlexRay buses; RS-232 and other UARTs; and rapid core-assisted debugging of designs that use Xilinx (www.xilinx.com) and Altera (www.altera.com) FPGAs. Other application-oriented features include segmented memory for analysis of laser pulses, radar bursts, and serial packets; offline PC viewing and sharing of previously acquired scope data; and RF-contextual viewing of scope data using vector-signal-analysis software.

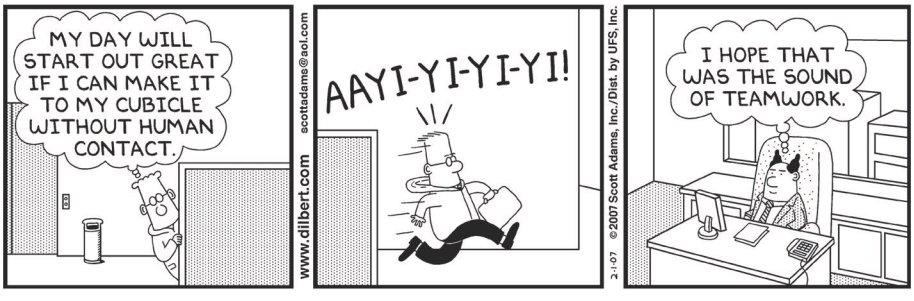
US prices for InfiniiVision DSOs and MSOs range from $6950 for a 350-MHz-bandwidth unit with two analog channels to $17,900 for a 1-GHz-bandwidth MSO with four analog channels and 16 logic channels. A 500-MHz DSO with four analog channels costs $11,050. All analog-only units contain the MSO hardware. To activate the MSO capabilities, you simply purchase a license.**—by Dan Strassberg**

▷**Agilent Technologies,** www.agilent.com/find/7000.



With a display whose resolution is greater than that of competitive instruments and whose area is more than 35% larger, the popularly priced InfiniiVision 7000 Series MSOs and DSOs provide a better view of your data. But the units' tour de force is their dramatically higher screen-update rates, which can bring elusive low-duty-rate phenomena to light in a tiny fraction of the time the competitive units require.

DILBERT By Scott Adams



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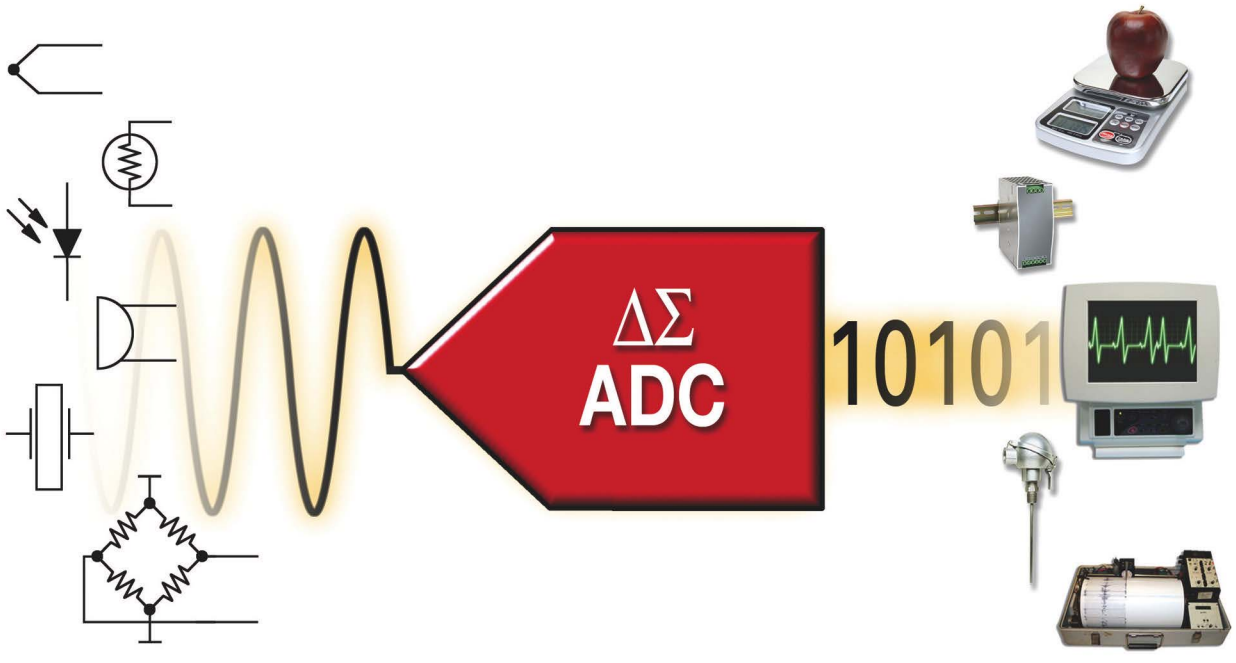

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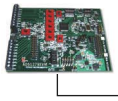
ADS1232	Ideal for weigh scales: 24-bit ΔΣ ADC, up to 23.5 effective bits, onboard PGA (G = 1, 2, 64, 128), 10SPS or 80SPS data rates
ADS1256	Best-in-class 23-bit, noise-free ΔΣ ADC: 8 channels, 30kSPS and programmable digital filter (averaging)
ADS1258	Fastest channel cycling, 24-bit, 125kSPS ΔΣ ADC: Measure all 16 channels in <675μs
ADS1278	Widest bandwidth, simultaneous sampling: 24-bit, 8-channel ΔΣ ADC, 128kSPS, 106dB SNR, ±0.0003% INL
ADS1281	Ultra-low distortion 24-bit ΔΣ ADC: 130dB SNR and –122dB THD while consuming only 12mW of power, ±0.00006% INL
ADS1610	Fastest 16-bit ΔΣ ADC: 10MSPS, 86dB SNR, 5MHz wide and flat bandwidth
DDC232	Highly integrated, current-input 20-bit ΔΣ ADC for measuring photodiodes, X-ray security and CT scanners: 32 channels



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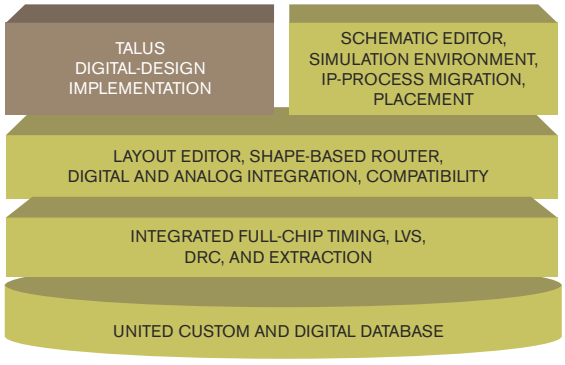
Texas Instruments

Magma takes on mixed-signal SOCs

Targeting consumer applications, SOCs (systems on chips) have in recent years integrated more and more analog circuitry. The circuits in question have been not merely the unavoidable PLLs and high-speed I/Os, but also control loops and precision signal paths spanning both audio and video. This situation has forced SOC designers into the world of mixed-signal design. To date, there have been two main approaches: One is to outsource the analog-block designs, import them again as hard IP (intellectual property), and hope that they work. The other approach is to use tool suites, such as Cadence's (www.cadence.com) Virtuoso, targeting skilled analog designers but integrating digital flows. This approach allows analog experts on the SOC team to do a custom analog design in the same database the digital folks are using for the rest of the SOC design, somewhat easing integration and verification.

Magma Design Automation recently introduced another alternative—one in keeping with the company's guiding concept that modest designs shouldn't require immodest expertise or license fees. The Titan platform will provide an environment in which not-full-custom analog design can proceed in parallel with digital design, merging during the physical design back end and working from a unified database. According to Ashutosh Mauskar, Magma's vice president of product and business development, Titan provides two paths by which a team can create analog designs. One is a schematic editor, from which the circuit description binds to foundry-device models to create a simulatable netlist. The other is an IP-oriented scheme, in which Magma defines commonly used analog functions in a topology template and a set of constraint equations. "The circuits will come right out of a textbook on analog design," Mauskar says, "so they will be familiar and useful."



The Titan platform integrates an approach to analog design with the Talus design flow.

The template-and-equation format allows Titan's process-migration tool to explore a range of alternative implementations in a new process technology within the constraints, offering designers their choice of migrated circuit designs. Thus, migrating an analog function in the Magma library to a new process node—although not exactly pushbutton—will be heavily automated. Working with the schematic and template tools, Titan will offer an analog-simulation environment that Magma based on the FineSim analog-placement tool. At this point, the isolation of the analog and digital designs ends, and both the simulated and placed analog netlist and the digital Talus netlist flow into a merged tool suite. That suite begins with a layout editor and a shape-based router that understands analog-circuit constraints, such as shielding styles and line-length control, preserving the operating characteristics of at least conservatively drawn analog circuits through the routing process.

The final stage in the flow is an extraction, timing, and checking stage. For this stage, Magma has incorporated its full-chip digital-timing tools: LVS (layout-versus-schematic) checking, DRC (design-rule-checking), and extraction. Although these concepts are familiar for digital designs, performing a full-chip LVS or extraction for an SOC with analog blocks is a different matter. LVS checking for analog circuits, for instance, requires rules decks from both the user and their foundry, according to Mauskar. Extracting analog components and model parameters from shapes is an unsolved problem, so the tools need this additional data. And extraction, which can use simple approximations for digital-timing purposes, also becomes far more complex in the analog domain. Magma employs a new transistor-level extraction tool based on the company's QuickCap capacitance extractor. Again, analog extraction is a work in progress, and future developments should use the detailed extraction algorithms that cell designers use.

All of the data for both the analog and digital nets goes into a unified database that complies with Open Access, reducing the version-control problems that can plague mixed-signal SOCs when the analog and digital designs proceed in isolation. The Titan approach addresses a number of the problems with mixed-signal SOC flows, but it is not a panacea, a universal custom design tool, or a substitute for having skilled analog designers, Mauskar warns. The template-based approach to analog-circuit design is more than adequate for normal, moderate-performance circuits, but it does not push a process node to its physical limits or implement science projects. It is for moderate-performance functional blocks. The migration tool also does not intervene in a circuit topology to find a better approach for a sigma-delta converter at 65 nm, for example. "The tools should work well with any technology node you can characterize accurately," Mauskar says. "But there is no way to replace human intelligence on the most demanding requirements. That's not what we are trying to do."

Magma is phasing the rollout of Titan over the course of the year. This quarter will see release of the Titan schematic capture, mixed-signal-layout and -routing, and chip-finishing tools. Magma will release the rest of the flow, including the analog-circuit templates and migration tool and the mixed-signal floorplanning tool, in beta form this quarter, and in production versions in the third quarter of this year.

—by Ron Wilson

▷**Magma Design Automation**, www.magma-da.com.

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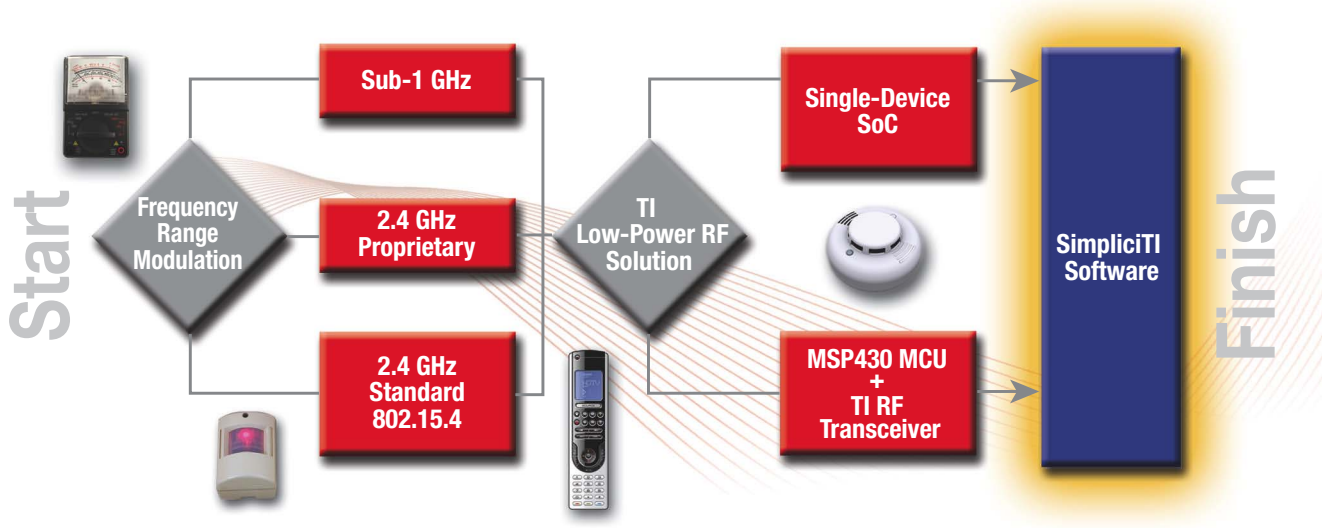

SimpliciTI is a low-power RF protocol aimed at simple, small RF networks. This open-source software is an excellent start for building a network with battery-operated devices using one of TI's low-power RF SoCs or the MSP430 ultra-low-power MCU and a TI RF transceiver. SimpliciTI network protocol supports alarm and security systems, automatic meter reading, smoke detectors, home automation and active RFID applications.

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CC2430	2.4 GHz System-on-Chip specifically tailored for IEEE 802.15.4 and ZigBee applications. CC2430 comes in three different flash versions, 8F, 16F and 32F, with 32/64/128 kB of Flash memory, respectively
CC2500	2.4 GHz RF transceiver designed for low-power wireless applications in the 2.4 GHz ISM band
CC251x	2.4 GHz, low-power System-on-Chip with integrated MCU, up to 32 kB Flash memory and optional full-speed integrated USB
eZ430-RF2500	USB stick-based development tool combining the ability of the ultra-low-power MSP430 with low-power RF transceiver in a single device

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Texas Instruments

Adaptive ICs optimize dc/dc-converter efficiency over wide load range

It can be a straightforward task to design a power supply for high efficiency at a single load point. Designing for high efficiency over a wide load range is a significant challenge, however. Organizations such as Energy Star (www.energystar.gov) specify minimum-efficiency levels of 100, 50, and 20% of full load for the ever-increasing minimum efficiencies that telecom and data-center computers require. Addressing this need, Zilker Labs' new ZL2004/2006 digital-dc-power controllers use proprietary algorithms to optimize converter efficiency over changing loads. Like the earlier versions of the converter family, the ZL2004/2006 features a digitally closed PWM (pulse-width-modulated) control loop.

The ZL2006/2004 uses proprietary control algorithms to optimize dc/dc-converter efficiency over widely varying loads.

These control-loop algorithms result in a full-load efficiency improvement as great as 3% and a light-load efficiency increase greater than 15% in typical applications, thus reducing peak power dissipation by as much as 20%. The chips automatically adapt their performance characteristics to increase the operating efficiency of the system when the load drops without sacrificing peak efficiency at heavy loads at which thermal concerns become important. The ZL2006 integrates 3A MOSFET drivers that can support loads in excess of 40A; The ZL2004 requires external-drive MOSFETs.

In addition to the adaptive-load algorithms, the ZL2004/2006 includes adaptive-diode emulation: As the load current falls, traditional synchronous step-down converters begin to sink current to maintain regulation, drawing current from the output capacitor and reducing efficiency. The ZL2006 and ZL2004 detect this point and prevent the lower MOSFET from turning on and pulling current from the capacitor, resulting in a 5 to 10% efficiency improvement at load currents of less than 1A. Another of the chips' means of increasing efficiency at light load levels is to reduce the operating frequency within a predefined range based on load-current changes.

> For higher currents, you can parallel multiple devices in a multiphase configuration.

For higher currents, you can parallel multiple devices in a multiphase configuration to achieve higher total load current than a single chip can support. As load demand decreases, the ZL2004/2006 can automatically optimize efficiency over the entire load range by turning off one or more phases in response to the load. Multiple devices can communicate through the single-pin digital-dc bus for nonhosted control of current-sharing and phase-sequencing. For a hosted power-management configuration, the chips support PMBus commands.

The ZL2006 has a 3 to 14V input range and a 0.54 to 5.5V output range and comes in a 6×6-mm, 36-lead QFN package. The ZL2004 has a 3 to 16V input range and a 0.54 to 4V output range and comes in a 5×5-mm, 32-lead QFN package. Prices start at $2.95 (1000).**—by Margery Conner**

▷**Zilker Labs**, www.zilkerlabs.com.

ADCs SHRINK IN SIZE, POWER FOR PORTABLE-SCANNER SOCKETS

Texas Instruments' analog-products group has introduced the ADS5281, ADS5282, and ADS5287 series of ADCs featuring 10- and 12-bit resolution and sampling speeds as high as 65M samples/sec. The units come in octal format–that is, eight per package–for compactness and low power consumption. The devices target use in medical imaging, such as ultrasound and MRI (magnetic-resonance imaging), wireless communications, military guidance, automatic-test equipment, and video.

At 65M samples/sec, the ADS5281 family uses 77 mW/channel. With dynamic scaling, at 30M samples/sec, the per-channel power drops to 48 mW. The chips interface directly with TI's recently introduced VCA8500 octal-variable-gain amplifier, which exhibits 0.8-nV/$\sqrt{Hz}$ input noise for a 63-mW-per-channel power consumption. The ADC-and-octal- amplifier pairing constitutes a complete medical-signal-chain device with better noise performance and lower power than alternative offerings, TI claims. Both parts come in 64-pin, 9×9-mm QFN packages for high-density systems.

The family of parts features a low-frequency noise-suppression mode that eliminates flicker noise, improving SNR (signal-to-noise ratio) by as much as 4.2 dB over a 1-MHz band in baseband and time-domain applications. Overload-recovery circuitry allows each ADC to provide valid data within one clock cycle after an input overload as high as 6 dB, allowing for immediate signal recovery and processing. You can program the devices' gain from 0 to 12 dB, driving full-scale outputs for input signals as low as 0.5V p-p.

TI also supplies the ADCs in an 80-pin TQFP that provides an easy transition to these next-generation devices, because it is pin-for-pin compatible with the previous-generation ADS527x family. Prices range from $40 to $68.60 (100), depending on speed and resolution. The octal amplifier costs $40.—by Graham Prophet

▶**Texas Instruments,** www.ti.com.

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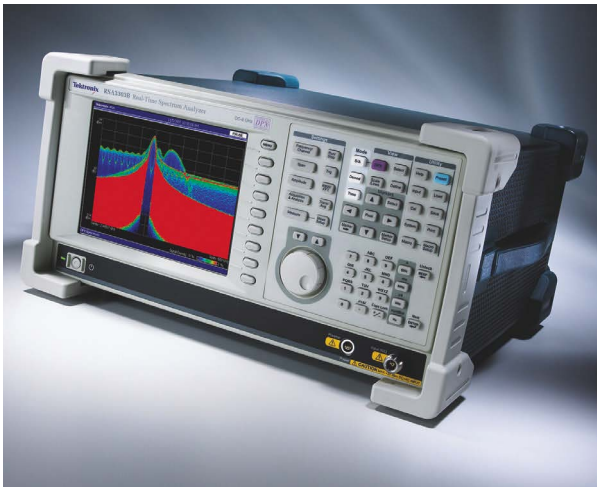
Agilent Technologies

Spectrum analyzer brings real-time analysis to midrange applications

Tektronix has announced the RSA3000B family of real-time spectrum analyzers, which bring the company's DPX waveform-image-processing technology to midrange spectrum analysis. The RSA3300B series and RSA3408B provide a live-RF view of the spectrum, enabling an unprecedented RF-signal-discovery capability for a broad range of digital-RF applications, including RFID (radio-frequency identification), mobile communications, and spectrum management. DPX rapidly transforms volumes of data to produce live-RF-spectrum displays that reveal previously unseen RF signals and signal anomalies.



The RSA3000B family leverages the manufacturer's DPX real-time-signal-processing technology—which, in spectrum analyzers had been available only in more expensive products—to present stunning displays that make short work of finding elusive anomalies in digital-RF spectra to 8 GHz.

The rapid expansion of digital-RF applications has driven the measurement needs of many applications beyond the capabilities of traditional swept-spectrum and vector-signal analysis. Digital-RF signals carry complex modulation that can change from one instant to the next, hopping frequencies, spiking briefly, and then disappearing. These transient and time-varying transmission techniques help RF devices to avoid interference, maximize peak power, and—often—evade detection.

According to Rick King, Tektronix's vice president of real-time-spectrum-analysis products, these analyzers are the first to solve problems that digital-RF technologies create. "Combining the high-performance RSA6100A series' DPX technology and live RF with a broad range of application-specific measurements makes the midrange RSA3300B series and RSA3408B the best choices not only for the toughest RF-discovery and -debugging problems, but also [for use as] as everyday spectrum-analysis and system-characterization tools," he says.

With a spectrum-processing rate hundreds of times as great as those of other vendors' spectrum analyzers, the new RSA3408B and RSA3300B-series units provide 100% probability of intercept for transients as brief as 31 and 41 μsec, respectively. The units combine the exclusive ability to trigger on transient signals in both the time and the frequency domains with unmatched troubleshooting and debugging of digital-RF designs.

The RSA3300B series is available with frequency coverage of either dc to 3 GHz or dc to 8 GHz. With 15-MHz capture bandwidth and 70-dB SFDR (spurious-free dynamic range), the RSA3300B units suit designing and debugging of 3G mobile systems; near-field systems, such as RFID and Bluetooth; and narrow- to medium-bandwidth communications systems. The RSA3408B covers dc to 8 GHz and provides 36-MHz capture bandwidth and 73-dB SFDR for applications that demand higher bandwidth and dynamic range, such as debugging of 3G mobile components and systems, design of WLANs (wireless local-area networks) and WiMax systems, demanding spectrum management, and general-purpose digital-RF debugging.

To display live spectra, the RSA3300B series' and RSA3408B's DPX waveform-image-processing technology uses dedicated real-time hardware to process more than 48,000 input-signal-spectrum measurements/sec—orders of magnitude more information than spectrum analyzers without a DPX display. This processing speed minimizes the analysis gaps inherent in swept-spectrum and vector-signal analyzers.

Besides live RF, the waveform-image processor provides an intensity-graded persistence display that holds anomalies until the eye can see them and shows the history of occurrences of dynamic signals, providing immediate feedback on signal variations over time. This display enables engineers to rapidly see transients and signals that are either completely invisible or that a user can deduce only after time-consuming offline analysis.

According to Tektronix, the 15-MHz-bandwidth RSA3000B and the 36-MHz-bandwidth RSA3408B are the only midrange spectrum analyzers that offer frequency-domain triggering. This function uses the FMT (frequency-mask-trigger) feature to find interfering and transient signals that no other instrument can, eliminating potential system instabilities from a design before they can cause problems. By displaying a seamless record of frequency and power changes over time, the new analyzers can solve transient problems, including modulation switching on software-defined-radio systems, identification of rogue pulses in radar transmission, and dynamic-modulation changes during a WLAN transmission.

The US suggested prices for the RSA3303B begin at $32,900; RSA3300B and RSA3408B software options handle 3G, WiMax, WLAN, RFID, signal-source, and general-purpose modulation and RF analysis.

—by Dan Strassberg

▷**Tektronix Inc,** www.tek.com/products/spectrum_analyzers/rsa3000.

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VOICES

Harley Feldberg: the pulse of the industry

Sometimes, the best way to get the pulse of the industry is to talk with electronics distributors who are out there on the street every day. Recently, *EDN* spoke with Harley Feldberg, president of Avnet EM (Electronics Marketing), about the economic situation, the growing role of Avnet in the design community, and the changing role of Asia in the industry. Portions of that interview follow. For more, go to ww.edn.com/article/CA6530480 and www.edn.com/080306p1.

Are you concerned about the economic slowdown?

A That's obviously the big question. I think the market, in lieu of good news, has been assuming bad news. The technology industry has been adopting a half-empty posture. After [our December analyst] conference call, we have one-on-one [calls] with the top analysts that follow our stock. That's where you get into the more meaningful questions and, in those one-on-ones, they generally asked, 'Are we concerned?' Of course we are concerned. All we can do because we are not economists, though, is relay what we are actually seeing. Now through the December quarter, we're just not seeing indicators [of a significant slowdown]. We're not seeing evidence of cancellations. We're not seeing unusual pricing pressure. It's really just a normal, rational market.

So, you have no concerns about inventory or lead-times with the economic situation?

A No. I think the only concern that I have is if we go into a severe global recession. Again, I'm not an economist, but we don't see that on the horizon. We really see pretty steady leadtimes, pricing, and demand. Are we concerned about the United States going into a gigantic recession that would impact citizens' purchasing of electronic things, which would impact our business in Asia? Of course we are. But at least through December, we don't see any indicators of that.

Are there any technology areas of special interest in the coming quarters for Avnet?

A We've been filling out our line card in two areas. One [is] where there are major suppliers that don't have a major presence in distribution but are important to our customers. We've been working with those guys. Our announcement about Maxim is a good example. [The company has] always been a valuable supplier to our customers but heretofore has not been a big participant in the channel. It's not a new product line to us, but it's a new way of doing business. It's an expansion with a large suppler that previously wasn't a player.

How important is Japan for Avnet's future growth?

A I always struggle to find a precise answer [to that question] because it is easy to be wrong. Numerically, as a market, it's a similar size to [that in the United States] and Europe, which makes it very attractive. Culturally, it's a market that does things differently from the West. So, if I've learned anything in the couple of years we've been focusing on Japan, it's patience. [Japan] is important, but it must be taken in the proper context. I wouldn't suggest we forecast 100% growth in 2008. We are growing, we're adding product lines, we are looking at potential acquisitions and partners, but I always temper those comments [by reminding people] that it's one [market] that requires time and patience. Ultimately, it will be a big market for us. The question is how long it will take.

You and Chief Executive Officer Roy Vallee have often spoken about balancing Avnet's growth globally. Yet it seems as though a lot of your business lately has been coming from Asia. Is this situation a red flag for you?

A Not really, but it is a reality that we have to accept and deal with. Currently, our business, if you average the last two quarters, is about 30% from Asia. If you contrast that to five or 10 years ago, it's grown dramatically. What we have said in the past is that we don't believe our business will mimic our suppliers' ratio. Most of our suppliers get more than 50% of their revenue from Asia. We think that, over the next two years or so, our business will be more like a third—35% or so. What that [situation] means is learning to deal in an environment of lower gross margins but higher asset velocity. Our ability to [increase] our operating-income ratio is going to be lower. It's going to continue to improve, but the rate at which it improves is going to be lower because we are starting from a lower gross margin in Asia. With that said, our preoccupation over the last five years or so on return on capital has really allowed us to get back to the right point. Our return-on-capital matches year on year have seen progress that's really phenomenal. It's really been a by-product of learning to do business in Asia—Asia-style. It means turning assets quicker, controlling costs more readily. It does mean a different model for us, but, so far, we've addressed it successfully.

Do you have any closing thoughts on the year ahead?

A It's a big question right now. Maybe we have quarterly amnesia. Maybe we have this conversation every quarter. But it does seem that, because of all the high-level concern about the macro market, we are all kind of on standby right now. What's the market going to do? Are we going to have a meltdown? We just don't see it, but I wouldn't want to be cavalier and suggest that we aren't watching it and aren't concerned about it. We will address whatever comes our way, but, for now, we feel pretty good about 2008.

—by Suzanne Deffree

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Too Hot or Too Cold May Be Just Right*

Q. Are absolute maximum and minimum temperatures as absolute as voltage or current ratings?

A. No! While integrated circuit manufacturers cannot guarantee devices used outside their temperature ratings, ICs do not suddenly cease to work beyond these limits. But engineers who choose to use ICs at other temperatures must determine for themselves how well they will work, and how consistent their behavior will be.

There are useful general rules. At temperatures around 185 to 200°C (the exact value depends on the process), increased leakage and reduced gain make silicon IC operation unpredictable, and accelerated dopant diffusion limits lifetimes to hundreds, or at best thousands, of hours. Nevertheless, ICs are regularly used at these temperatures in applications, such as drill head instrumentation, where degraded performance and reduced lifetime are acceptable. At slightly higher temperatures, though, operational lifetimes may become too short to be useful.

At very low temperatures, reduced carrier mobility eventually causes devices to stop working, but some circuits will function, albeit out of specification, at temperatures below 50 K.

Basic physics is not the only limiting factor. Design compromises may improve performance in one temperature range at the cost of malfunction outside it — the AD590 temperature sensor, for example, works in liquid nitrogen if it is powered and then cooled, but will not start at 77 K.

More subtle effects result from performance optimization — the commercial grade of a device (0 to 70°C) may have very good accuracy within this temperature range, but dreadful accuracy outside it, while the military grade (–55 to +155°C) of the same device may maintain

slightly lower accuracy over the wider temperature range because of a different trimming algorithm, or even from a slightly different circuit design. The difference between the grades may not only be due to different testing.

Two other issues are the behavior of the package material, which may fail before the silicon, and the effects of thermal shock — the fact that an AD590 will work at 77 K if cooled slowly does not mean that it will survive the high transient thermo-mechanical stresses of suddenly being plunged into liquid nitrogen.

The only way to use a device outside its specified temperature range is to test, test, test, and test again, thus ensuring that you understand how the non-standard temperature affects the behavior of devices from several different batches. Check all your assumptions.[1] The IC manufacturer may or may not be helpful and will probably not give any guarantees for out-of-temperature operation.

* *"The Goldilocks Enigma" by Paul Davies ISBN 0547053584*

[1] *"Check your assumptions. In fact, check your assumptions at the door." 'Barrayar' by Lois McMaster Bujold ISBN 2290313157*

To learn more about temperature ranges

Go to: http://rbi.ims.ca/5704-101

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Have a question involving a perplexing or unusual analog problem? Submit your question to:

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BY BONNIE BAKER

Delta-sigma ADCs in a nutshell, part 4: noise versus data rate

This article is the last in a brief overview of the inner workings of delta-sigma ADCs. You have seen how the modulator operates in the time and the frequency domains and how it shapes the conversion-quantization noise into higher frequencies. The modulator implements an oversampling system that has an integrator and negative feedback. You've also read about the inner workings of the digital/decimator filter. This filter reduces the high-frequency noise in the digital 1-bit stream from the modulator while passing the digitized input signal to the converter output at a reduced data rate. The combination of these two modules yields a high-resolution ADC (**references 1**, **2**, and **3**).

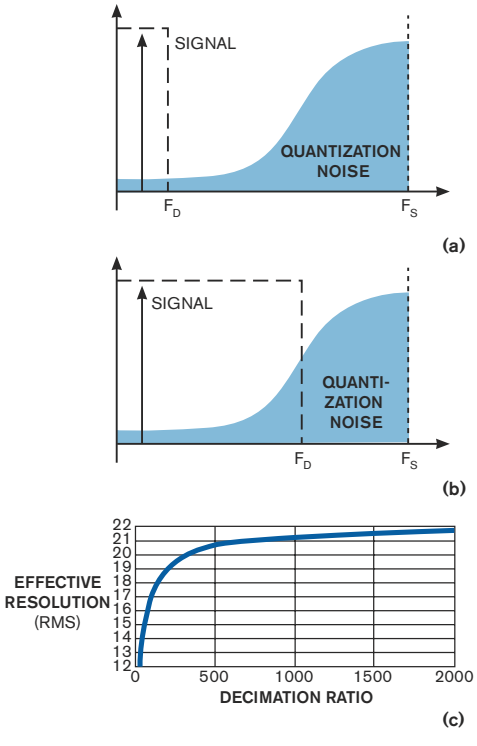

Figure 1 Decreasing the output data rate (a) or increasing the decimation ratio (b) produces a conversion with a higher effective resolution (c).

With any converter, the actual resolution is equal to the number of bits the ADC transmits. "Effective resolution" describes the useful bits from an analog-to-digital conversion as they relate to signal noise. Effective resolution is equivalent to the ADC's effective number of bits. The ratio of the modulator's F_S (sampling rate) and F_D (output-data rate) define the decimation, or oversampling, ratio, which directly impacts effective resolution. The decimation ratio, whose value ranges from four to 32,768, equals the number of modulator samples per data output.

Consider the frequency spectrum in **Figure 1**. Suppose that you make the output data rate a small fraction of the modulator's sampling frequency (**Figure 1a**). The input frequencies from zero to F_D are in the output-signal band. The effective resolution is high because the noise level is low. A higher frequency for F_D increases the converter's output-data rate and decreases the effective resolution. Most of the noise from the modulator is in the higher frequencies, but you still have a lower effective resolution (**Figure 1b**). **Figure 1c** shows an example of the relationship between decimation ratio and effective resolution of a sampling ADC.

One way to increase the output-data-rate speed without changing the effective resolution is to increase the modulator-sampling rate. You can increase this rate by increasing the master clock rate to the delta-sigma ADC. With a constant decimation ratio, both the sampling rate and the power consumption increase. Also, most converters have a practical limit for the sampling rate, beyond which they do not function properly. A strong relationship exists between the decimation ratio and effective resolution. Keeping the sample rate constant and lower data rates gives you high effective resolution at the output of the converter (**references 4** and **5**).EDN

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Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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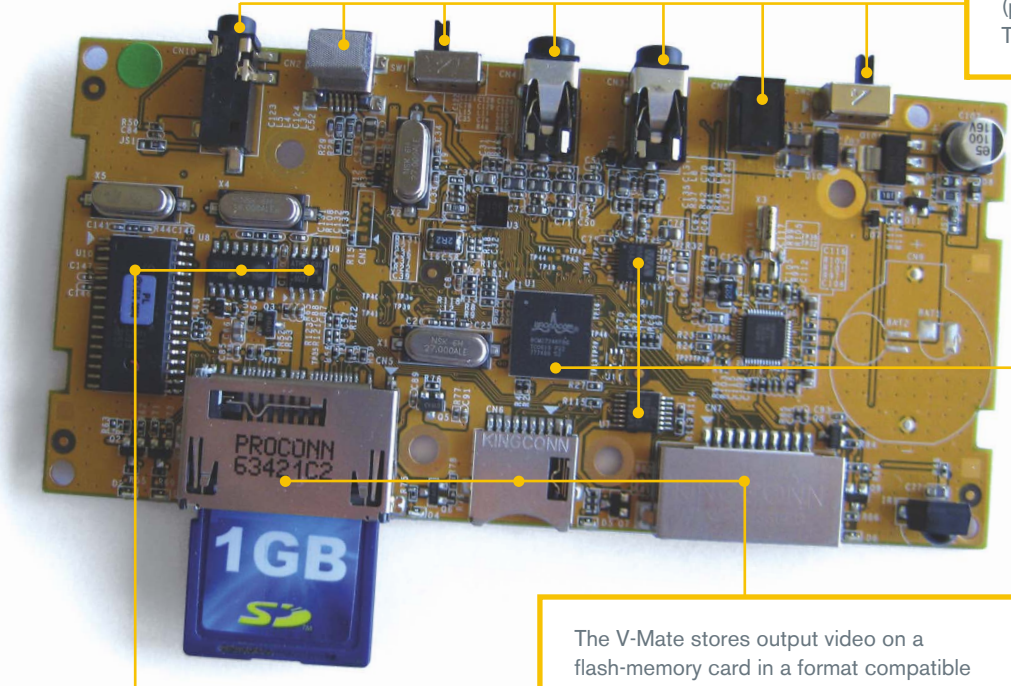
SanDisk V-Mate video-memory-card recorder

SanDisk's V-Mate video flash-memory-card recorder records video to flash cards from TV, cable, and satellite set-top boxes, and DVD or VCR players, to play back on mobile phones, PDAs, handheld game consoles, and video/music players. A remote-control- and TV-based graphical user interface let users control settings and recordings and access content. It has multiple programming slots for entering channel, date, and start/stop times to schedule recordings. At initial setup, users select their playback device, such as a mobile phone or handheld game, to ensure that the recordings are playback-compatible. Recording time is approximately 3.6 hours in a mobile phone at a bit rate of 544 kbps and 1.8 hours on a notebook computer at 1.056 kbps. The V-Mate measures 5.1×2.6×0.8 in. and costs $80 to $120.

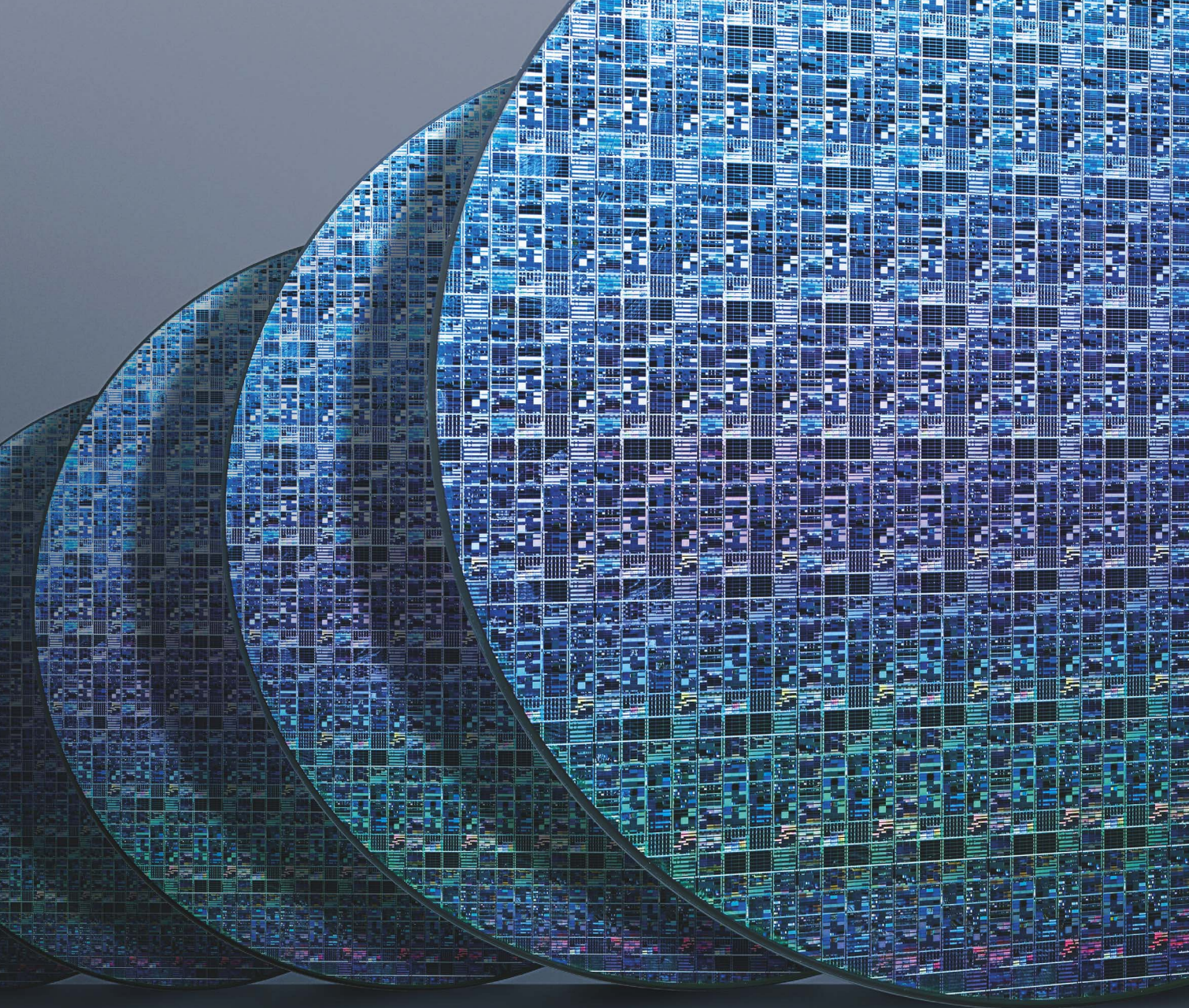
The V-Mate connects in the analog-signal line between the set-top box and the TV using component-video and -audio connectors. The device comes with two cables that combine the three-component signal lines into a single 3.5-mm connector to match the small V-Mate panel space. It also comes with an infrared emitter and cable to send commands to the set-top box. The V-Mate includes only a power switch and a switch to select PAL (phase-alternating-line) or NTSC (National Television System Committee) format.



The V-Mate employs a number of integrated devices for the mobile market, resulting in a small, low-power unit. The Broadcom BCM2724 and support chips form the heart of the unit and feature MPEG-4 VGA or H.264 CIF (common-intermediate-format) video encoding/decoding at 30 frames/sec, plus TV output. The BCM2724 integrates 64 Mbits of embedded SDRAM with the Broadcom VideoCore multimedia processor, enabling software implementation of the full range of multimedia codecs. In the same board area, the Wolfson Microelectronics WM8960 low-power stereo codec integrates a microphone interface and a stereo-headphone driver. Targeting portable digital-audio applications, the device provides on-chip digital-signal processing for automatic level control for the line input.

The operator interface is through the remote control and TV screen. The user can select the transcoding format and set up recording schedules by following on-screen prompts. The device implements the infrared interface section with an 8-bit MDT10P55 microcontroller from MDT, an AT24C01 serial EEPROM from Atmel, and infrared codes from Universal Electronics. The unit also includes an infrared emitter that automatically turns on the cable-, satellite-, or terrestrial-TV tuner box and selects the channel.

The V-Mate stores output video on a flash-memory card in a format compatible with the user's mobile device. SanDisk's Web site lists more than 140 compatible portable devices, including PDAs; several versions of the Apple iPod; and cell-phone models from Motorola, LG, Nokia, Palm, Samsung, Blackberry, Siemens, and Sony Ericsson. Some devices, such as the Apple iPod, without a plug-in flash-memory card, require an extra memory-copy step. The device supports SD (secure digital), MMC (multimedia card), MMCplus MMCmobile, SDHC (secure digital high capacity), MiniSDHC, MicroSDHC, Memory Stick Pro, Memory Stick Duo, and Memory Stick Pro Duo.



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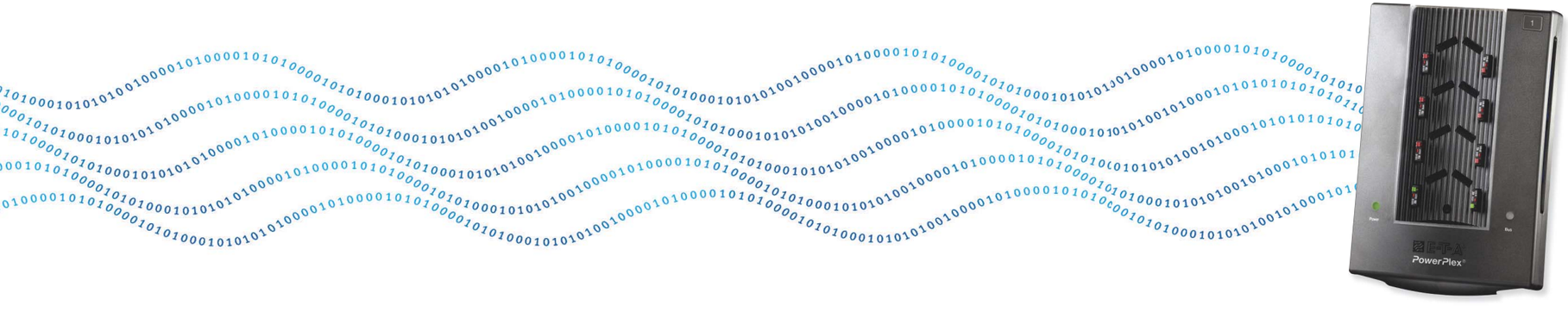

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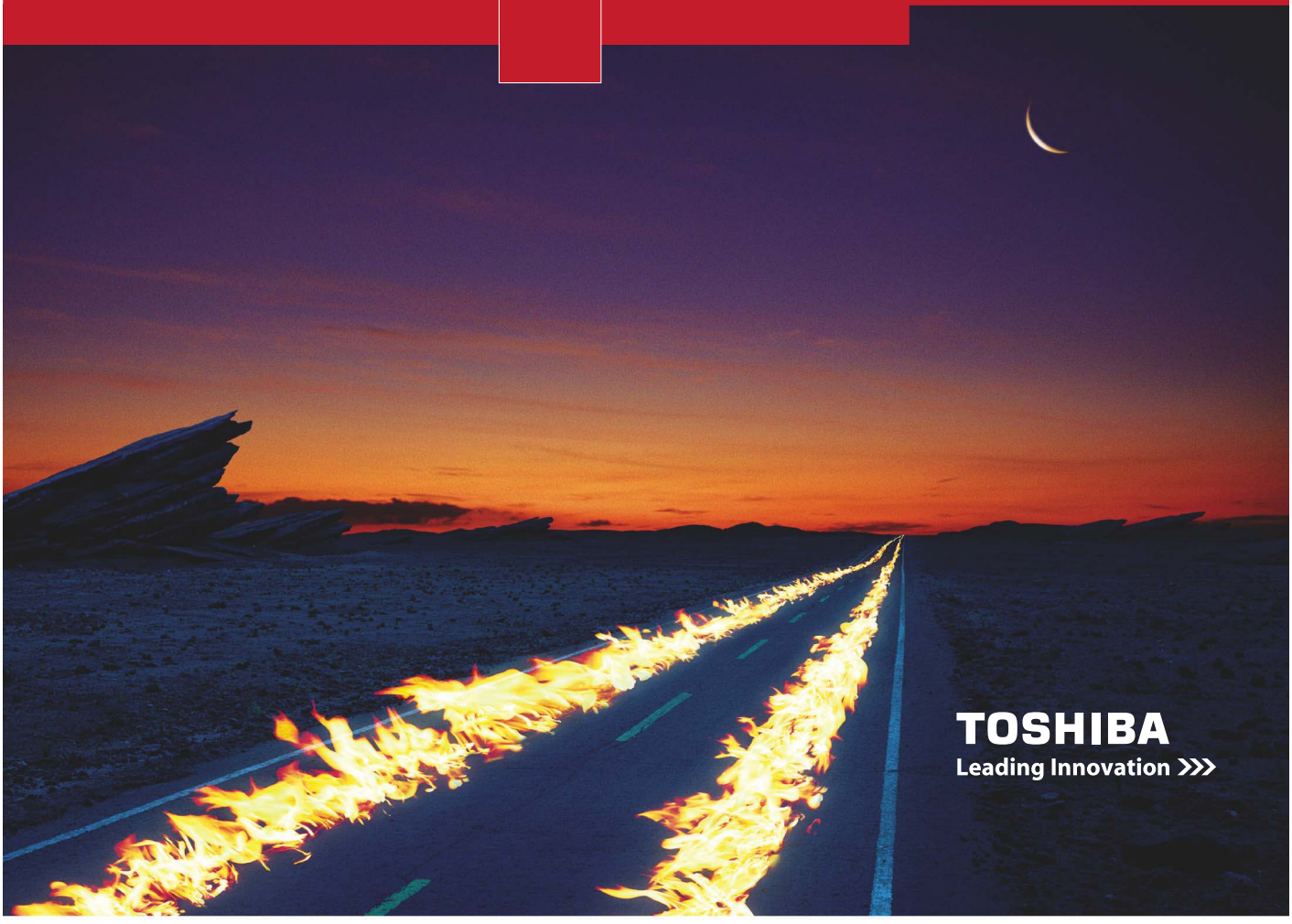


INDUSTRY INITIATIVES, SUCH AS THE GREEN GRID AND CLIMATE SAVERS, HAVE SET THE AMBITIOUS GOAL OF HALVING DATA-CENTER ENERGY USAGE BY 2011. TO ACHIEVE THIS OBJECTIVE, THE INDUSTRY MUST SHIFT TO THE USE OF DIGITAL-POWER CONTROL AND MANAGEMENT AT THE AC/DC- AND DC/DC-POWER-SUPPLY LEVEL. A SHIFT TO DC-BUS-POWER DISTRIBUTION WITHIN THE DATA-CENTER INFRASTRUCTURE ALSO SHOWS PROMISE.

Eltek Valere's Flatpack2 HE 48/2000 rectifier module offers 96% typical power-conversion efficiency, which the company claims is the highest efficiency level available.

PUSH FOR POWER EFFICIENCY

FORCES CHANGES IN SERVER-CENTER HARDWARE AND SOFTWARE

BY MARGERY CONNER • TECHNICAL EDITOR

Advances in server-processing power have coupled with increasing demands on workloads to drive up data-center power consumption in the United States. Currently, data centers, or server "farms," account for 1.5% of the total US electricity bill, and that figure should rise to nearly 3% by 2011 (**Reference 1**). In addition, data-center-electricity costs now outpace hardware costs over the four-year life of a server. Purchasers of servers, who previously pinched pennies when specifying server hardware, now are open to spending a little more for hardware if a more sophisticated and efficient power-supply design will yield lower power bills. The need to reduce electricity costs and the desire to responsibly use energy have made power efficiency at the hardware, software, and infrastructure levels a top priority for data centers. And, because data centers are among the largest end applications for power supplies, their needs will influence the agenda for designers and manufacturers of power supplies.

The US government's EPA (Environmental Protection Agency) encourages data-center efficiency through efforts such as Energy Star, which has just released the first draft of its "Program Requirements for Computer Servers" (**Reference 2**). Industry groups such as the Green Grid and Climate Savers are developing guidelines for best practices, promulgating new technologies, and generally shining the light on the need for greater power efficiency in businesses.

Until recently, the data-center industry focused on leveraging facility space rather than power usage. As servers got smaller in size and cost, their physical facility's price and maintenance remained the same or increased. Thus, it made sense to cram as many servers as possible into each facility. However, a by-product of operating a server is heat: For every watt a server processor consumes, it wastes another half-watt in cooling; ac/dc- and dc/dc-power conversion and regulation cost another half-watt. As long as energy costs were relatively low, it made sense to solve

the cooling problem by using air conditioners. As energy costs soared, however, this approach became economically and environmentally impractical.

This concern for power efficiency is relatively recent in the data-center world, according to Tom Darby, who manages Texas Instruments' data centers and is the company's representative on the Green Grid. As an example, he points out that IT (information-technology)-industry trade shows once focused on increases in server-processing speeds and capability. In the past year, however, the trade shows have shifted their focus onto power efficiency—to the extent that an EPA director gave a recent keynote speech. "Green" technology may be a nice-to-have feature in many parts of the US economy. For the data-center sector, however, cost savings due to energy efficiency has become a dominant force, affecting hardware design and even placement of the data center itself. For example, one of the key reasons for Google's decision to start a data center in The Dalles, OR, was the community's proximity to cheap hydroelectric power.

The power-supply community has for several years been discussing a move to digital power. In particular, digital control of the PWM (pulse-width-modulated) control loop has struggled to catch on in the power-supply industry, especially the "silver-box" ac/dc-power supply that powers every rack of servers in a data center, because of the price sensitivity of these supplies. Even 50 cents' worth of additional parts is enough to put a silver-box supply out of the competition, and digital-power controllers can add a couple of dollars. In addition, an analog-control loop tuned for a specific load can perform as well as a digital-control loop. Combine greater cost, brand-new technology that's alien to analog designers, and no clear technological advantage; it's no wonder that digital power has not taken off in the silver-box-supply market.

AT A GLANCE

- Data-center efficiency now consumes 1.5% of the total US electrical power.
- Data-center operators are willing to pay a premium for power-efficient hardware.
- Although it holds promise, dc-power distribution requires a major change in the power infrastructure.

However, the quest for improved efficiency will drive the adoption of digital power in server applications because the power supply must be able to maintain a high efficiency over not just one load, but a range of loads. Analog loops can't provide a high efficiency over loads that can range from 20 to 100% of full load.

Servers must respond over such a widely varying load because the vital nature of a data center's workload requires redundant power supplies to serve as backups for each rack of servers. Both of the redundant supplies operate at 50% of the load under normal conditions, with the load varying from 100 to 10% or less depending on the workload and power-supply status. Achieving efficiency over such a wide load swing is difficult with an analog-PWM-loop supply, but a digitally closed loop can tune itself for changes in the load and make efficient operation possible over the load range.

Just a few years ago, the cost savings due to increased power efficiency wouldn't have been enough to offset the higher cost for parts. Now, IC vendors are eyeing the greater complexity as a way to justify higher IC costs. For example, Analog Devices recently introduced its first digital-power-controller IC and pointed out that it supports a complicated design such as that in **Figure 1** (**Reference 3**). The circuit increases a converter's efficiency by as much as 1%—enough to get the attention of power-supply designers. Analog Devices officials hope that the ability to support the new two-stage design will be a plus for the chip.

Digital power also confers the ability to communicate with individual supplies both within and among server racks. Power-supply-system management requires intelligence within the power supply to self-monitor heat, operating time, and load response. Digital-power ICs offer a range of power-management options, including a host-controlled system, such as a PMBus-(power-management-bus)-based controller or Power-One's Z-One digital-power-management system. These power-communication buses require a separate intelligent host that can query supplies about their operating time, heat, and fan response, and they can also sequence supplies down

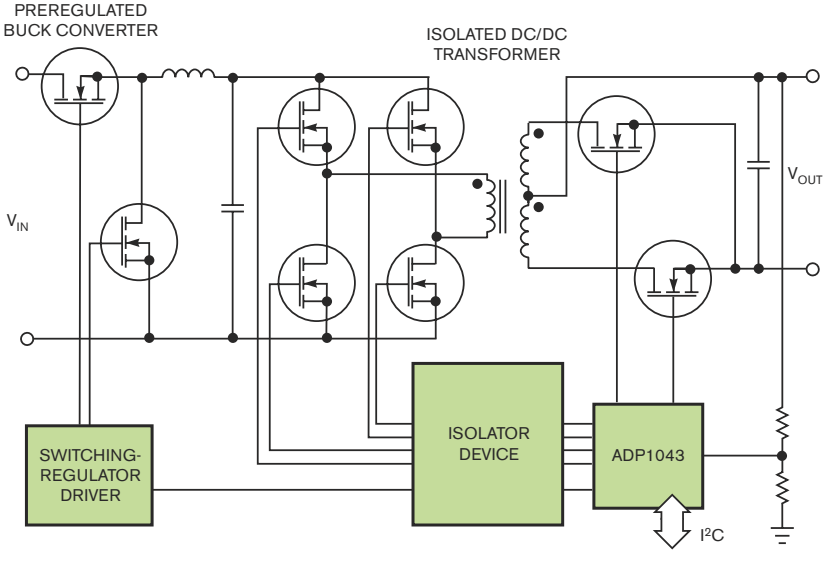
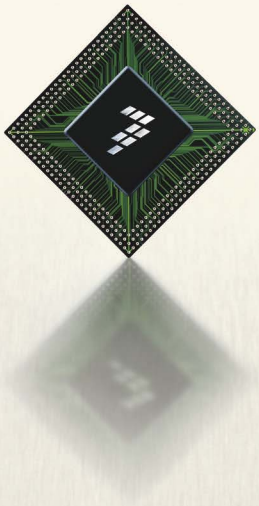


Figure 1 Digital-power controllers, such as Analog Devices' ADP1043, can simplify the incorporation of complex new-circuit designs within server power supplies. This two-stage dc/dc-controller design must drive and control seven FETs but can result in a power-supply efficiency increase of 1%. The design takes the input voltage from the power-factor-correction output bulk capacitor and buck-converts it down to a lower regulated voltage. The isolation stage now runs as a high-efficiency dc/dc converter running in an open loop.



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or up. The controllers can also store information about the power system to schedule maintenance before a failure. Not all systems require such elaborate control. For example, some digital-loop power controllers can also communicate between controllers in a simpler no-host-control scheme that may provide enough control for some systems. For example, Zilker Labs' ZL2006 and 2004 controllers allow communication between chips without a host or a communication bus.

In addition to increasing power-supply efficiency, data centers can optimize system power efficiency through software virtualization of hardware servers. With virtualization, a server can support several jobs at once, rather than dedicating one physical server to a job regardless of whether the job requires the server's entire processing bandwidth. In effect, virtualization subdivides the physical server into multiple virtual machines until no excess processing capacity remains on the server. With the advent of server virtualization, a system host requires no dedicated server: If a hosting system requires only some of a hardware server's bandwidth, the rest of the bandwidth can host one or more separate systems, depending on the hardware's capacity and the bandwidth needs of the hosting system.

According to Kevin Bross, modular-systems architect at Intel, a data center responding to a recent virtualization survey reported that virtualization had allowed a 10-to-1 reduction in the number of servers and a 2-to-1 reduction in the total power usage because the remaining servers were receiving heavier usage.

Although using digital power and virtualization are two relatively straightforward power-reduction tools, the third tool, using a dc-power-distribution bus, requires changing a basic part of the data-center infrastructure. Current methods involve twice converting data-center power to dc: This approach converts power as it enters the center to power the UPS (uninterruptible power supply) system and then converts the power back to ac for distribution through the building to the rows of server racks. This ac-to-dc-to-ac conversion shuffle causes the loss of approximately 20% of a data center's power.

One of the first companies to announce an infrastructure-level dc-voltage plan is Validus DC Systems. The Validus system's basic architecture calls for the conversion of ac power to −575V dc where it enters the building at a power-quality-module air-cooled rectifier. The −575V dc routes through the facility through a power-distribution module, a scalable "switchboard" that integrates power distribution from multiple system inputs, such as the utility, a UPS, or battery banks. Also at this point, alternative-energy sources, such as solar- or wind-generated power, can enter the power-distribution scheme. The power switchboards integrate and distribute the high-voltage dc to the power-converter units for each row of server racks and convert −575V-dc to −54 V-dc power, distributing as much as 120 kW to the server row.

Ron Croce, chief operating officer at Validus, says that the company has received an increasing number of inquiries from data-center operators interested in power distribution for alternative energy, which is often dc. Validus' switchboard approach lends itself to paralleling the output of photovoltaic systems to boost the dc power to usable distribution levels, he says. In addition, few data-center operators would want to rely

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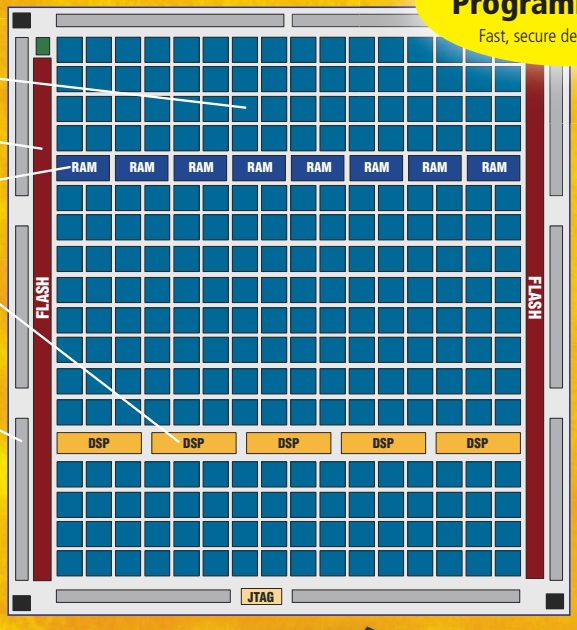

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at least initially on a purely alternative-energy source. Validus' approach allows the integration of several power sources, allowing a data center to use, for example, dc-photovoltaic power during the day and switch to ac-grid power at night. Over a five-year period, the total cost of ownership, including equipment, installation, maintenance, and efficiency saving, yields a 50% savings over a conventional ac approach, according to Croce.

Intel's Bross points out that using a dc-voltage bus for power distribution is tried-and-true method within the telecom industry, in which −48V dc is the norm. Pragmatically, Bross suggests that, rather than getting into unending discussions about the practicality of dc power within the data-center industry, engineers can make extensive evaluations with currently available telecom equipment. He goes further than just pointing out dc power's practicality, however. He also offers a sophisticated online calculator that allows facility engineers to perform side-by-side evaluations of the efficiency of ac-power-system power versus that of −48V-dc power systems. The calculator does not rely on generalized assumptions about the efficiency of a UPS or the gauge of a distribution cable. It instead allows you to plug in your own numbers for every piece of the complicated power-distribution and -conversion puzzle. Check out the ac-versus-dc-power calculator for yourself, and you'll see the difference dc-power distribution makes: It's a winner (**Reference 4**). For example, Eltek Valere's Flatpack2 HE 48/2000 rectifier module offers 96% typical power-conversion efficiency, which the company claims is the highest efficiency level available. Prices begin at $450.

Steve Oliver, vice president of marketing and sales for Vicor's VI Chip, agrees that −48V dc holds promise for energy-efficient power routing and points out that a move to dc power also brings up the opportunity to rethink power distribution within server racks and servers. Oliver says that, when converting from an intermediate 12 or 9.6V rail to the load, designers often use a synchronous-buck converter. With this topology's duty cycle, the higher the input voltage relative to the output voltage, the worse the circuit's efficiency. For example, a synchronous-buck-rectifier circuit that drops 12V down to 6V has an efficient 1-to-1 duty cycle. But a circuit that drops 12V down to 1V requires a less efficient 1-to-12 duty cycle; it also stresses the switching and control FETs. Oliver sees a move away from synchronous-buck converters and toward circuits and devices that can efficiently make the drop from 48V to less than 1V with little or no loss in efficiency. Vicor's VI chips can make the drop from 48V to, for example, 0.8V in one stage, he claims.

Although servers do need higher voltage rails to power devices such as disk drives, 90% of a large system's load powers the processor with 0.9V and the memory stack with approximately 1.2V. Oliver suggests a hybrid power architecture that includes a main power unit on each server going from 48V down to the low processor and memory voltages and a much smaller supply handling vestigial higher voltage rails. **EDN**

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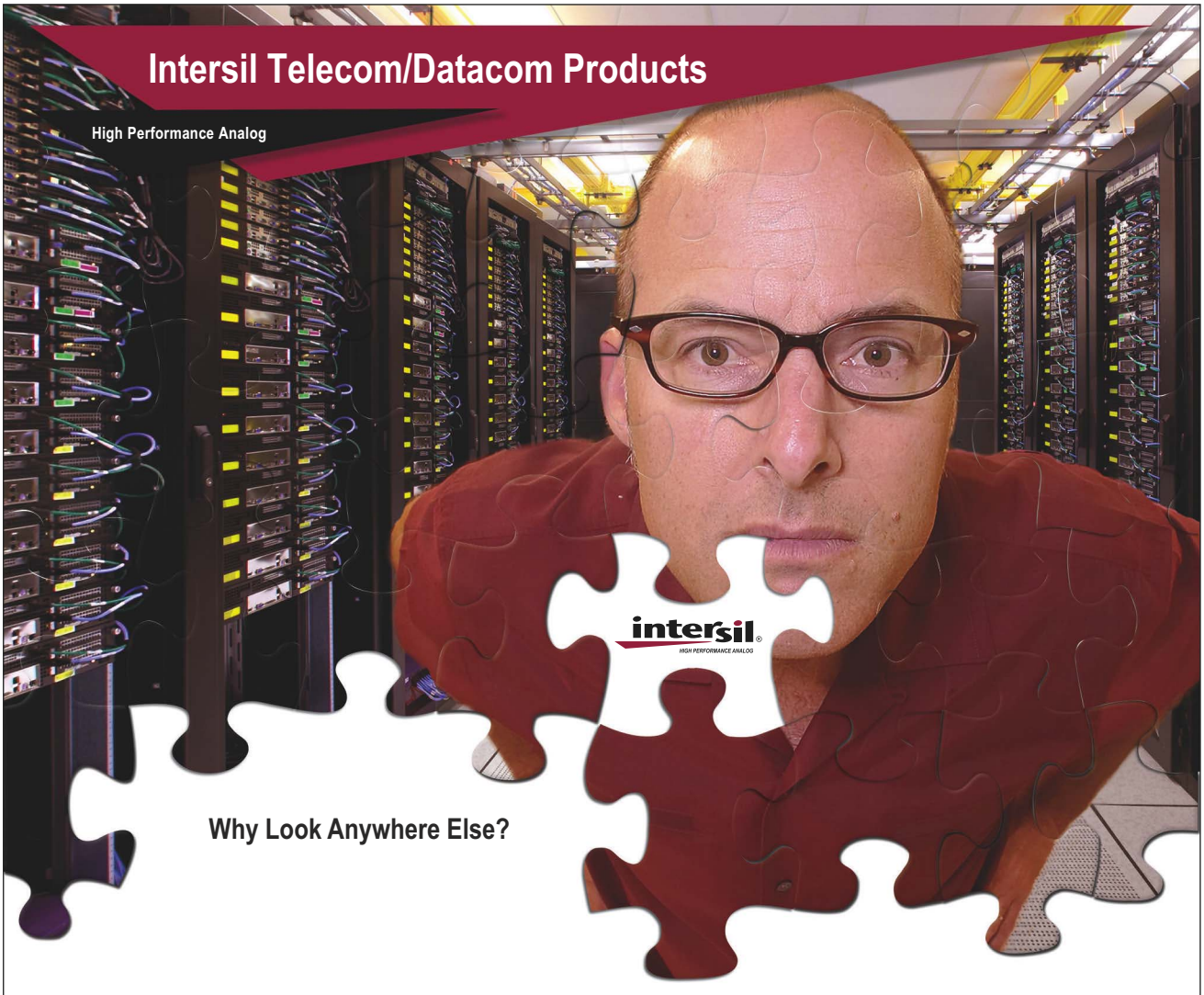

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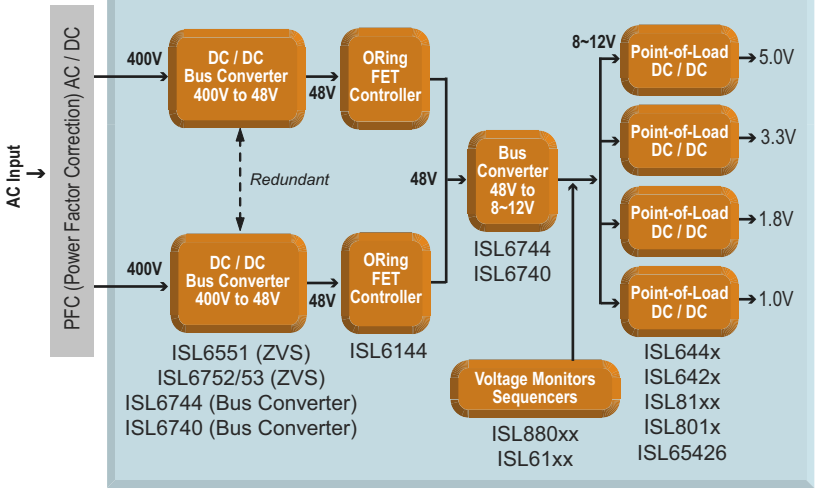

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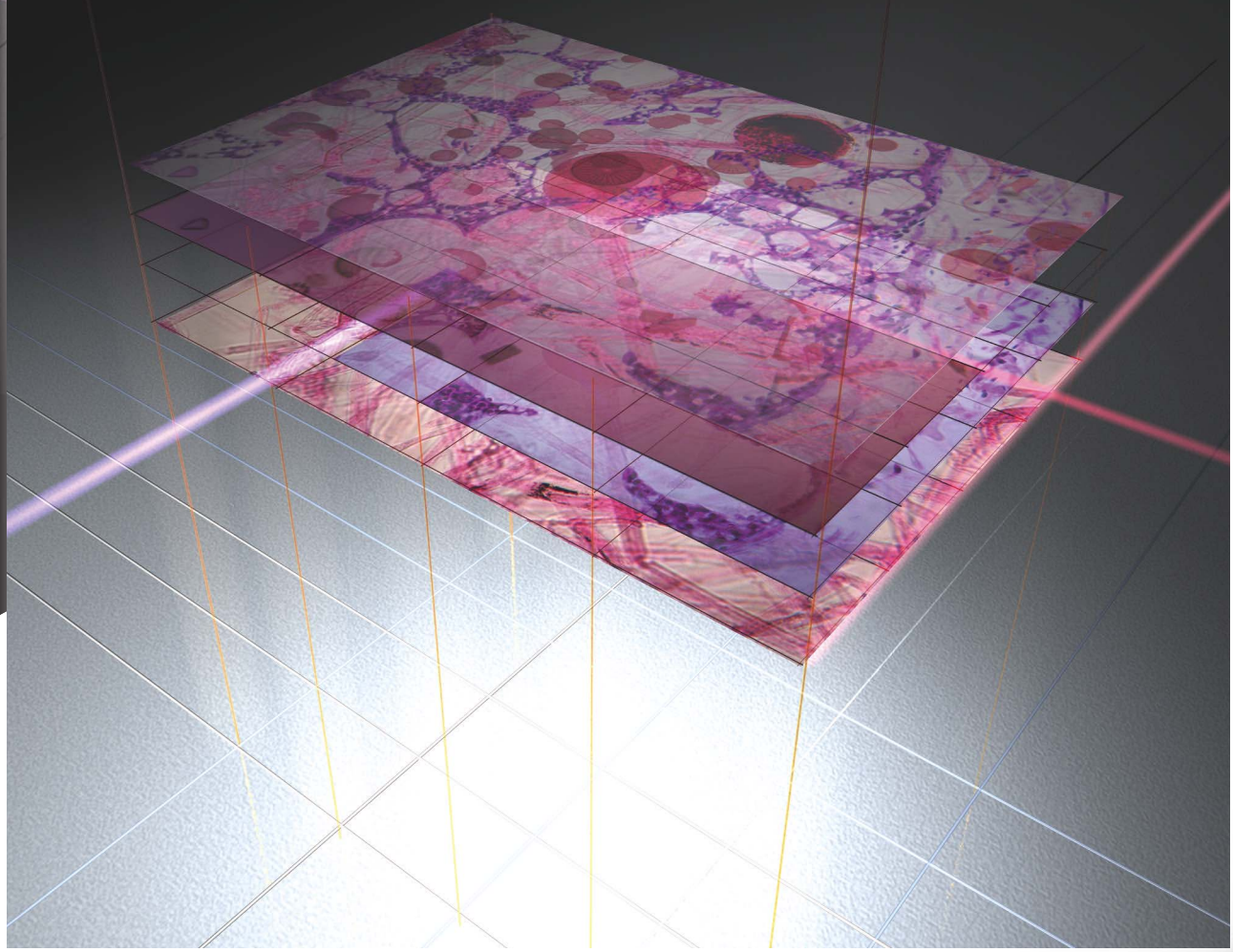
The 2008 EDN DSP directory

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

THIS YEAR'S DIRECTORY CAN HELP YOU TO PEEL AWAY THE LAYERS OF COMPLEXITY TO FIND THE PERFECT DIGITAL-SIGNAL PROCESSOR FOR YOUR PROJECT.



Welcome to the 2008 *EDN* DSP Directory, which again groups an ever-expanding list of digital-signal-processing resources in a single repository. The number of companies, devices, cores, and offerings in the directory continues to evolve and grow. Once again, a few companies have dropped off the list, and new companies have replaced them. This continuing increase in processor vendors is a testament to the variety of available processing options and the tremendous variation among requirements, features, and applications for which designers use these devices and cores.

This year's directory includes the increased presence of multiple-core offerings similar to those that disappeared from the directory a few years ago. One difference between now and then is that these multicore architectures are not merely IP (intellectual-property) cores for licensing, but they exist as silicon products from companies such as Stream Processors and Tilera.

A key aspect of these multicore offerings is how the processing performance can scale beyond a few cores, through lanes or mesh architectures, and how developers can use normal software-programming tools to efficiently use the on-chip resources of these devices. Will this iteration of multicore architectures that can scale processing performance to dozens or potentially hundreds of cores survive the real-world development demands of the market? Stay tuned for future editions of the directory to find out.

In the meantime, the directory continues to aim to provide designers and system architects with enough visibility into processor options to quickly narrow the list of candidate processors and enable the exploration of multiple approaches for each project. The print version offers a quick and high-level overview of the digital-signal-processing industry by identifying what is new at each company and what applications each company's product lines target. As always, our Web site expands the material you find in the print version.

The online "Where did they go?" section helps you find companies that we no longer list because they are out of business, other companies have acquired them, or they've failed supply us with the updated information we needed for this year's directory. The section includes data from previous years to make it possible to track this type of data without having to locate earlier versions of the directory.

The Web version expands greatly on the print edition. It offers not only the print material, but also device **tables** and detailed pages dedicated to each company's devices, cores, development tools, and other product offerings. The detailed device pages support a top-level taxonomy that allows you to find the devices by vendor and by application. They also include architectural block diagrams, if available, for each vendor's offerings.

If you cannot find a company in the directory, or if a company did not participate in the update, please let the company and *EDN* know that you missed reading about them in the directory. Likewise, if this directory helps you find or choose a device or core, please let the vendor know how you found its part.

Help us continue to make the directory better by visiting us at www.edn.com/dspdirectory and by sending your comments and feedback to dspdirectory@edn.com.

ACTEL CORP, WWW.ACTEL.COM

Actel offers single-chip, nonvolatile FPGA technologies along with signal-processing capabilities, such as filtering and domain conversion. The company's DirectCore system-level IP (intellectual-property) blocks target use with its FPGAs, such as the RTAX-S and ProASIC3 device families. When you implement the flexible IP cores in Actel's flash- and antifuse-based FPGAs, they are immune to firm errors and tolerant of radiation. The company's devices support a live-at-power-up feature, which allows them to target military, communication, aerospace, and medical applications that require no power-up delay.

ALTERA, WWW.ALTERA.COM

Altera's portfolio of FPGAs, structured ASICs, and CPLD products targets many electronics markets. Building on the Stratix device family, the 65-nm Stratix III FPGAs incorporate features, including dedicated DSP blocks, to combine high performance with the lowest possible static- and dynamic-power consumption; these new devices improve performance by as much as 50% over previous-generation high-end FPGA devices. Stratix III FPGAs include programmable-power technology; selectable core voltage, process, and circuit technologies; and support from the Quartus II PowerPlay power-analysis and -optimization technology. The 65-nm Cyclone III FPGAs with 288 embedded multipliers for DSP applications target high-volume applications requiring low power, high performance, and low cost.

AMI SEMICONDUCTOR, WWW.AMIS.COM

AMI Semiconductor supplies integrated mixed-signal and structured-digital products that target the automotive, medical, industrial, communications, and military/aerospace markets in North America, Europe, and the Asia Pacific region. The company's BelaSigna product line of ultra-low-power audio-processing systems targets portable-system applications, such as mobile handsets, headsets and headphones, industrial hearing protection, and ALDs (assistive listening devices).

Innovations for the BelaSigna 200 and BelaSigna 250 DSP-based system-on-chip audio-processing systems include an echo-cancellation algorithm that provides clear, echo-free audio in office-telecom headsets and wireless mono and stereo headsets. The company also introduced a 5×5-mm BelaSigna 250 package.

ANALOG DEVICES, WWW.ANALOG.COM

Analog Devices' DSP offerings include the Blackfin, SHARC, and TigerSHARC families of processors. The Blackfin processor family combines a 32-bit RISC-like instruction set with 16-bit dual MAC (multiply/accumulate) units and targets convergent applications with audio-, video-, and data-processing requirements. The devices' dynamic power-management enables lower power consumption by supporting the simultaneous adjustment of system operating frequency and voltage under application control.

The SHARC-processor family targets applications ranging from consumer, automotive, and professional audio, to industrial, test and measurement, and medical equipment. The 32-bit floating/fixed-point core architecture includes a sophisticated memory and I/O-processing subsystem.

The TigerSHARC-processor family offers high-density floating- and fixed-point performance. It supports glueless-multiprocessor scalability, targeting wireless-communications-infrastructure, medical-imaging, industrial-imaging, and military applications.

Analog Devices' SigmaDSP audio processors provide a single-chip audio system with a 28/56-bit audio DSP, ADCs, DACs, and microcontroller-like control interfaces. Signal-processing elements include equalization, crossover, bass enhancement, multiband dynamics processing, delay compensation, speaker compensation, and stereo-image widening, which you can use to compensate for the real-world limitations of speakers, amplifiers, and listening environments.

ARC INTERNATIONAL, WWW.ARC.COM

ARC International offers two configurable, 32-bit processor-core families that use a 16/32-bit ISA (instruction-set architecture) providing both RISC and DSP capabilities in a unified architecture. The ARC 600 targets battery-operated and cost-sensitive products in the embedded-control, consumer, networking, and automotive markets. The ARC 700 delivers computing performance targeting graphics, media, packet processing, and high-end embedded platforms using operating systems such as Linux. ARC also offers the ARC XY advanced DSP-memory subsystem, which adds a complete DSP engine to ARC CPU cores and enables conventional and signal-processing computation within a single unified architecture.

ARM, WWW.ARM.COM

ARM licenses semiconductor IP (intellectual property), including processors, peripherals, interconnect and physical libraries for the development of complex SOC (system-on-chip) devices. ARM processors target automotive, consumer-entertainment, imaging, networking, storage, security, and wireless-system applications, and ARM bases them on a common architecture that emphasizes performance, low power consumption, and reduced system cost. The company offers the ARM7, ARM9, ARM10, and ARM11, as well as the Cortex family of processors featuring Thumb-2 technology and the SecurCore-processor family. ARM's DSP-enhanced cores support products that require a mixture of DSP and control functions on a single core. ARM Neon technology provides powerful, flexible acceleration for media and DSP applications; ARM OptimoDE data-engine technology targets power-efficient, deeply embedded signal-processing applications; and the ARM9E processor family targets products for microcontroller DSP and Java applications.

ATMEL, WWW.ATMEL.COM

Atmel's bases its DSCs (digital-signal controllers) on the AVR32 UC3, AP7, and ARM926EJ-S cores. Atmel also offers the dual-core, VLIW (very-long-instruction-word), floating-point Diopsis DSPs, which it based on the company's complex-domain, GFLOPS Magic DSP core coupled with an ARM microncontroller unit. The 220 freely intermixable, 16- and 32-bit extended instructions that the UC3 DSCs support include single-cycle MACs (multiply/accumulates), multipliers, atomic-memory ma-

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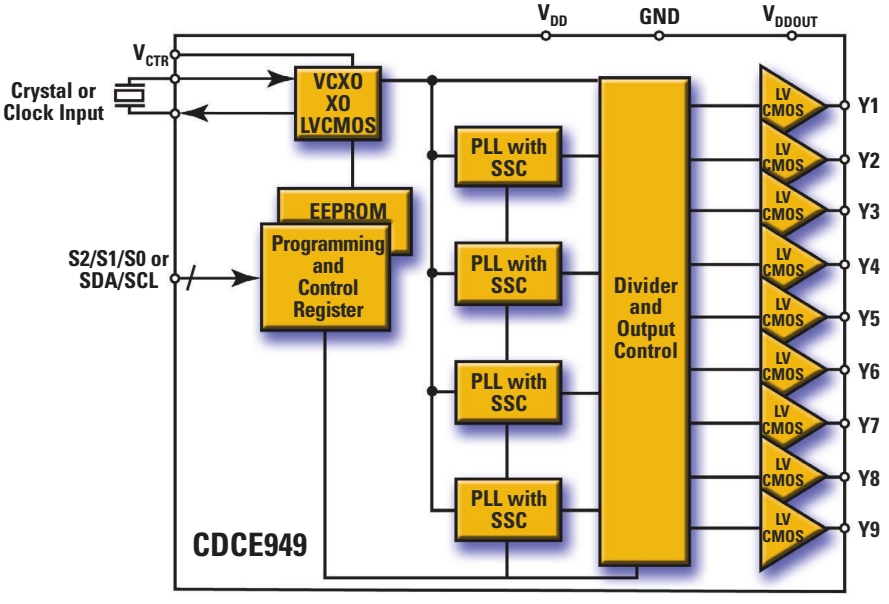

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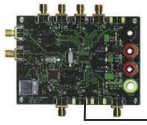
CDCE925	1.8	2.5/3.3	2	5	230	–40 to +85	16
CDCE913	1.8	2.5/3.3	1	3	230	–40 to +85	14
CDCEL949	1.8	1.8	4	9	230	–40 to +85	24
CDCEL937	1.8	1.8	3	7	230	–40 to +85	20
CDCEL925	1.8	1.8	2	5	230	–40 to +85	16
CDCEL913	1.8	1.8	1	3	230	–40 to +85	14



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CAMBRIDGE CONSULTANTS, WWW.CAMBRIDGECONSULTANTS.COM

For more than 45 years, Cambridge Consultants' expertise has ranged from semiconductors, wireless communications, radar systems, advanced sensors, and control systems in automotive electronics, medical devices, and consumer goods.

The company's portfolio of IP (intellectual-property) and development tools includes an extensive library of analog, digital, mixed-signal, and wireless-IP cores together with embedded-software-development and debugging tools, protocol stacks, and design platforms for ASICs and FPGAs. The IP cores are portable and flexible, and designers can tailor them to their specifications with flexible licensing contracts that can be royalty-free. Cambridge Consultants' silicon-IP offering includes 16- and 32-bit XAP-processor cores and the APE2 configurable datapath DSP.

CEVA, WWW.DSP.COM

During the year, the Ceva the Ceva-TeakLite-III DSP Core, a third-generation DSP core it based on the TeakLite DSP architecture. This feature-rich, native-32-bit architecture is backward-compatible with previous versions of Ceva-TeakLite cores and delivers higher performance for less power for applications such as HD (high-definition) audio for home entertainment and audio processing for high-end-multimedia devices. The company also enhanced the Mobile-Media portable multimedia platform, with support for the RealVideo and VC-1 video formats. Mobile-Media is configurable for end markets ranging from low-cost, video-only applications through complete multimedia products for high-resolution-media products.

Ceva licenses a family of synthesizable, programmable DSP cores; DSP-based subsystems; and application-specific platforms. The Ceva-X DSP architecture supports features and capabilities for advanced signal-processing requirements, including 3G/3.5G/WiMax (worldwide-interoperability-for-microwave-access) baseband and video, audio, and VOIP processing.

CHIPWRIGHTS, WWW.CHIPWRIGHTS.COM

Fabless-semiconductor company Chipwrights offers DSPs for audio-, video-, and image-processing applications. The company's processor family combines a 32-bit RISC-like serial-application processor with an array of 32-bit, MAC (multiply/accumulate), ALU (arithmetic-logic-unit), and shift parallel processors. The parallel, scalable architecture enables greater data processing than conventional single- and dual-core devices with fewer cycles and less power consumption.

This year, Chipwrights introduced the CW5631, which combines an ARM-926EJ-S processor with a 16- or 32-bit (CWVx) parallel processor and a serial-application RISC processor with enhanced-video I/O ports, high-speed USB, I^2S/AC97 audio, CompactFlash, a 10/100-Mbit Ethernet interface, and SD (secure-digital)/MMC (multimedia-card) interfaces.

CIRRUS LOGIC, WWW.CIRRUS.COM

Cirrus Logic offers DSPs targeting audio applications. The company's portfolio includes single-core and multicore DSPs for consumer markets as well as CobraNet audio-system processors for professional, commercial, and consumer markets, featuring Cirrus Logic's CobraNet technology for delivering uncompressed digital audio over Ethernet networks.

CLARKSPUR DESIGN, WWW.CLARKSPUR.COM

Clarkspur Design offers 16-, 24-, and 32-bit DSPs. Its emulator boards support USB-cable controls, and the company offers license-free audio-compression programs, such as Ogg Vorbis.

CRADLE TECHNOLOGIES, WWW.CRADLE.COM

Fabless-semiconductor company Cradle Technologies develops multicore DSPs targeting next-generation multimedia-system applications. Cradle delivers high-performance, scalable, programmable DSP platforms for video and imaging in security and surveillance, high-performance imaging, and broadcast and IPTV (Internet Protocol-televsion) head-end-infrastructure applications. The CT3616, Cradle's flagship multicore system, can provide real-time encoding of Main Profile H.264 at D1 resolution on one chip.

EVATRONIX, WWW.EVATRONIX.PL

Evatronix offers IP (intellectual-property) cores and electronic-design services, including a range of processor, USB, serial-interface-controller, data-communication, and networking cores. It also offers two families of programmable DSP cores. The 16-bit C32025 family targets industrial, home, and consumer applications, and the 24-bit C56000 core targets more complex applications requiring high accuracy, such as audio compression and image processing.

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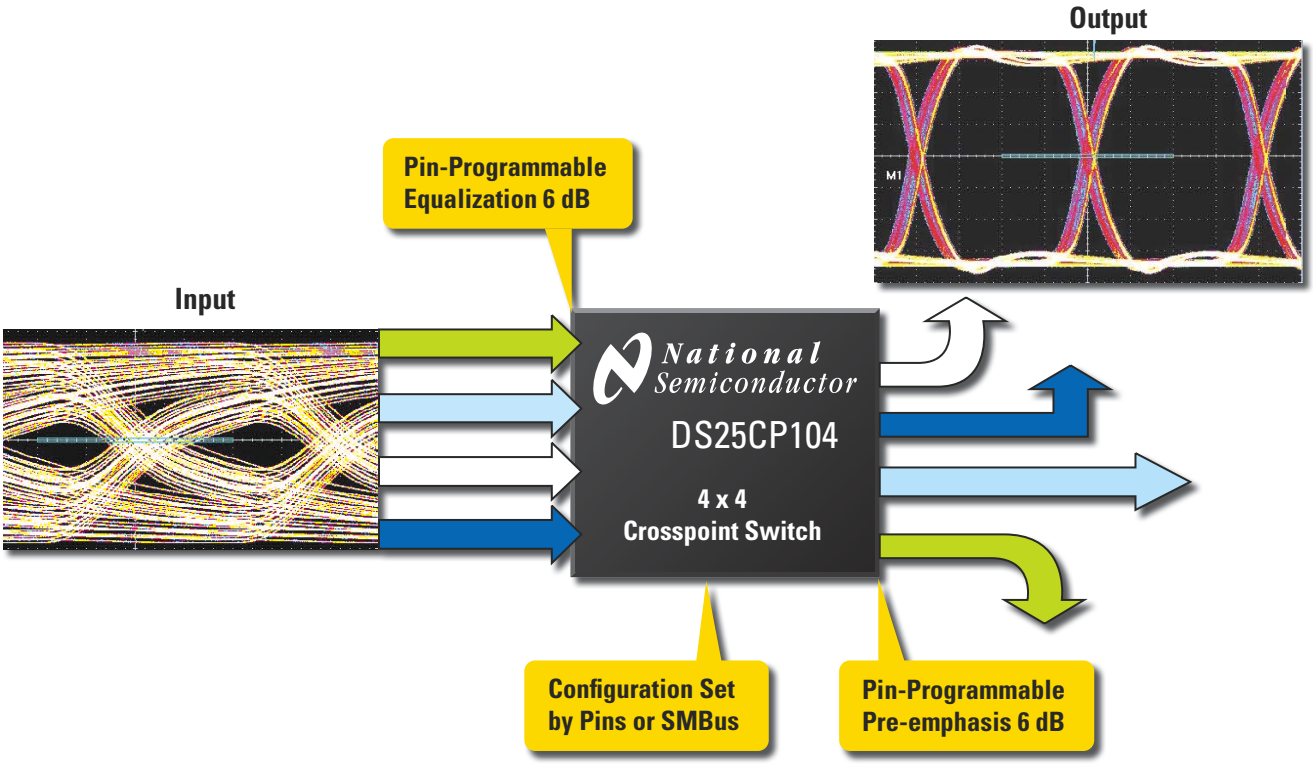
Energy Efficient 4x4 DS25CP104 Crosspoint Switch with Equalization



DS25CP104 Features

- 3.125 Gbps max data rate
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- I_{CC} 37 mA per channel (typ)
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- Crosspoint configurable using external pins or SMBus
- Available in LLP-40 packaging

LVDS Crosspoint Switches

Product ID	Function	Max Datarate	Features	Power
DS25CP152	2 x 2	3.125 Gbps	Pre-emphasis, 8 KV ESD, Equalizatin	211 mW
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Applications

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FREESCALE SEMICONDUCTOR, WWW.FREESCALE.COM

Freescale Semiconductor offers programmable DSPs that target audio, mobile-handset devices, and advanced communications-infrastructure equipment. The quad-core MSC8144 is the company's highest performing programmable DSP. The MXC architecture, which integrates StarCore DSP technology, targets 2.75G and 3G mobile applications. The Symphony family of audio DSPs targets high-fidelity professional-, consumer-, and automotive-audio applications.

Freescale also offers DSCs (digital-signal controllers) that combine the computational power of DSPs with the ease of use and control functions of microcontrollers in single-chip devices for motor control, digital-power conversion, and lighting-control applications.

Last year, the company introduced a voice-enabled GPON (gigabit-passive-optical-networking) SOC (system on chip). Delivering gigabit line-rate packet forwarding, the MSC7120 integrates a StarCore DSP, an e300 CPU built on Power Architecture technology, and a datapath engine to deliver a complete PON (passive-optical-network) subsystem in a single device.

NEW GENNUM, WWW.GENNUM.COM

Gennum designs and manufactures semiconductor products for global video, data-communications, and audio markets. The Voyageur DSP targets high-quality-audio and related applications that demand ultra-low-power consumption, programmable flexibility, and compactness. The multiprocessor platform has a reconfigurable architecture that integrates high-resolution ADC and DAC peripherals that are available in miniature packages. Voyageur's reconfigurable, multicore system comprises hard-wired accelerators and five DSP cores; four of the DSP cores are dual-MAC (maultiply/accumulate)-unit cores with a customized instruction set for audio processing, including single cycle logarithmic and exponential functions. Voyageur contains FFT/IFFT (fast-Fourier-transform/inverse-FFT) accelerators, hard-wired filter-engine blocks of FIR (finite-impulse-response) and IIR (infinite-impulse-response) filters, and a perfect-reconstruction programmable time-domain filter bank for subband audio processing.

HYPERSTONE, WWW.HYPERSTONE.COM

Hyperstone's processors provide integrated RISC/DSP functions for applications requiring a high-speed microprocessor with a high-performance DSP. These processors feature dual execution units in a pipelined architecture sharing registers. They can mix RISC- and DSP-specific programming transparently to the programmer. They execute RISC/DSP instructions with a high degree of parallelism, resulting in high throughput.

IMPROV SYSTEMS, WWW.IMPROVSYS.COM

Improv Systems offers the Jazz PSA (programmable-systemarchitecture)platform, a configurable, multiprocessor architecture that allows designers to create their own application-based optimized processor cores. Improv's VLIW (very-long-instruction-word) Jazz-processor architecture employs parallel execution of operations, targeting computationally intensive applications, such as media processing, digital-signal processing, and communication. The fixed-point Jazz cores target general DSP applications.

Improv also offers preconfigured cores that are complete hardware and software implementations for high-growth, emerging markets. Jazz Media cores include video-, audio-, image-, and speech-processing implementations targeting consumer-electronics devices ranging from mobile handsets and portable media players to high-definition digital displays. Jazz Voice cores address the needs of the voice-over-packet market, including all points of the voice network.

INFINEON TECHNOLOGIES, WWW.INFINEON.COM

Infineon Technologies offers 8-, 16-, and 32-bit microcontroller families offering DSP capabilities. The 8-bit XC800 family incorporates a Vector Computer unit that suits sensorless-field-oriented-control applications. The 16-bit XC16x family, with integrated MAC (multiply/accumulate) and CapCom6E units, targets motor-control schemes, such as constant VF, frequency slip, and field-oriented control. The 32-bit TC116X family, which Infineon bases on the TriCore unified-microcomputer/DSP architecture, targets applications such as servo control, audio-domain digital-signal processing, data communications, modems, automotive systems, and portable systems.

In 2007, Infineon introduced two 16-bit families it based on the C166S V2 core. The XE166 RTSC (real-time signal controller) and the XC2000 have a normal instruction set for general task control and a MAC (multiply/accumulate) instruction set dedicated to DSP and 32-bit mathematical operations. The XE166 RTSCs can simultaneously control as many as four motors. The XC2000 family addresses the complexity of automotive applications from body and gateway applications to air bags, electronic power steering, and power trains.

IPFLEX, WWW.IPFLEX.COM/EN

IPFlex offers dynamically reconfigurable processors and design-tool platforms targeting imaging and video, communication/wired, medical, and automotive applications. The company's DAP-DNA (digital-application-processor/distributed-network-architecture) incorporates a RISC processor as a controller with a heterogeneous matrix of 300 to 1000 processing elements. The DNA architecture can reconfigure within a single clock cycle to deliver flexible, field-programmable, and high-performance processing. IPFlex offers the DAPDNA-2 and DAP-DNA-IMS (Internet-multimedia-subsystem)-product lines. DAPDNA-IMS products target imaging and video applications, and DAPDNA-2 products target multiple purposes and applications.

LATTICE SEMICONDUCTOR, WWW.LATTICESEMI.COM

Three of Lattice Semiconductor's 90-nm FPGA families will interest DSP designers. The recently introduced LatticeXP2 family combines flash configuration memory, LUT (look-up-table) logic, embedded memory, and DSP blocks to enable single-chip, secure, and instant-on FPGAs. The LatticeXP2 devices provide as many as 40,000 LUTs, 32 18×18 multipliers, and 885 kbits of embedded memory. Lattice also offers the low-cost LatticeECP2 and LatticeECP2M FPGA families, which include as many as 100,000 LUTs, 168 18×18-bit multipli-

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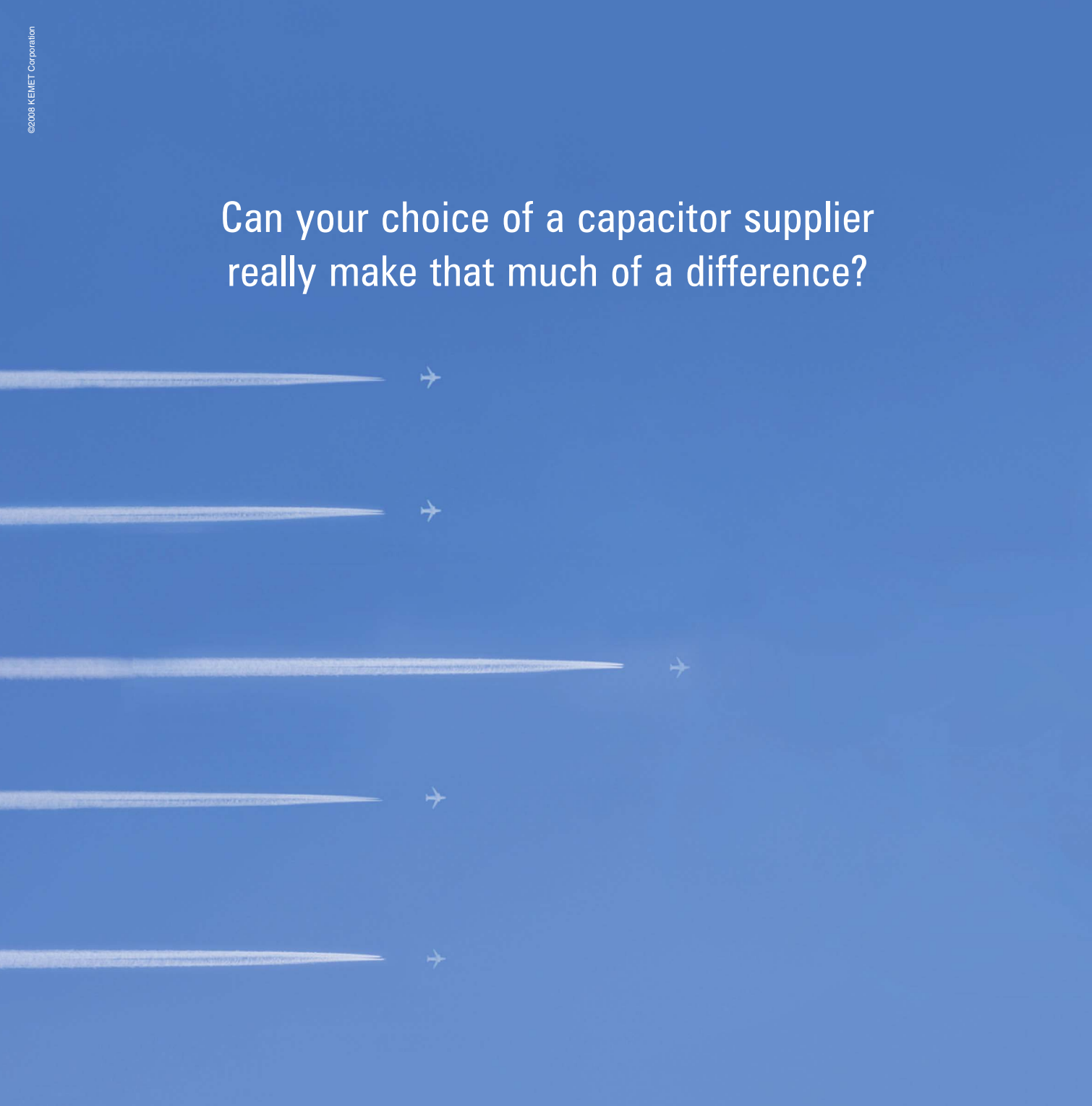

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LSI LOGIC, WWW.LSILOGIC.COM

See the "Where did they go?" section at the online version of this article at www.edn.com/dspdirectory. VeriSilicon acquired LSI Logic's ZSP division.

MICROCHIP TECHNOLOGY, WWW.MICROCHIP.COM/DSPIC

Microchip's dsPIC DSC (digital-signal controller), a 16-bit (data) modified Harvard RISC machine, combines the control advantages of a high-performance, 16-bit microcontroller with the high computation speed of a fully implemented DSP to produce a tightly coupled, single-chip, single-instruction-stream option for embedded-system design. All of Microchip's 16-bit DSC and microcontroller-unit families share the same core instructions, peripherals, and development tools, and they have compatible pinouts. DSCs add DSP instructions.

During the year, Microchip released 18 devices in the 40-MIPS dsPIC33F family. Standouts include four dsPIC33 DSCs, such as a family for a new class of smart-sensor processing and a family to execute sensorless control of the most advanced and energy-efficient motor types, as with Microchip's free field-oriented-control algorithm. Additionally, Microchip added three motor-control and three general-purpose, low-pin-count dsPIC33 DSCs that feature as much as 32 kbytes of flash memory in packages as small as 6×6 mm. The dsPIC33F family continues to grow with flash memory ranging from 12 to 256 kbytes, pin counts of 18 to 100, and a number of peripheral configurations.

MIPS, WWW.MIPS.COM

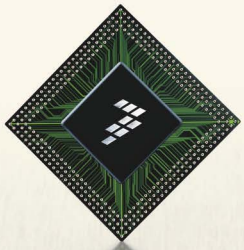
MIPS Technologies offers a comprehensive line of processor cores that it bases around a processor architecture used in DTV (digital television), broadband access, WiFi, cable-set-top boxes, DVD recorders, HD (high-definition) DVDs, and VOIP (voice-over Internet Protocol) applications. The fully synthesizable, 32-bit MIPS32 74K cores can achieve operating frequencies greater than 1 GHz in 65-nm process. The MIPS DSP ASE (application-specific extensions) Revision 2 includes 74 built-in DSP instructions that can eliminate the need for a separate DSP core.

MORPHO TECHNOLOGIES, WWW.MORPHOTECH.COM

Morpho Technologies focuses on processing engines for software-defined radio. Its MS2, a platform for ultra-low-power software-multimode radio, targets applications such as handsets. In addition, Morpho licenses a WiMax (worldwide-interoperability-for-microwave-access)-system product through integrated hardware and software IP (intellectual property), and it includes the MS2 PHY (physical)-layer communications engine.

NXP SEMICONDUCTORS, WWW.NXP.COM

NXP Semiconductors' Nexperia family of media processors targets connect-



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ed multimedia products in the mobile-wireless, audio, imaging and video, and consumer markets. Forming the DSP component of the Nexperia brand is NXP's Adelante technology, which includes the classic 16-bit RD1602x and 24-bit RD2412x DSP cores with a user-definable VLIW (very-long-instruction-word) architecture. The high-performance Adelante VD3204x embedded-vector DSP family rounds out NXP's offering. With its innovative vector-processing architecture, which minimizes power consumption, the VD3204x targets computationally intensive functions in communication and broadcast-reception applications. Adelante provides its DSP technology with the Adelante software-development kit, a verification environment for multicore SOC (system-on-chip) architectures.

NEW OCTASIC, WWW.OCTASIC.COM

Octasic offers DSP-silicon devices and software for the converged carrier, enterprise, and endpoint-communication-equipment markets. Its Vocallo multicore-media-gateway DSP, which the company introduced last year, is a next-generation platform that targets voice, video, and data-over-IP (Internet Protocol) applications. The hardware and software platform allows media-gateway developers to match an offering to their requirements. Vocallo allows designers to add their own software to the framework to differentiate their products.

ON DEMAND MICROELECTRONICS, WWW.ODM.AT

ODM (On Demand Microelectroncs) offers IP (intellectual property) and SOCs (systems on chips) targeting the upcoming global digital-video revolution. The basis for ODM's product portfolio is the silicon-proven VSP (video-signal processor)—a scalable, configurable, and fully software-programmable processor. The VSP handles applications with extremely high-performance demands, such as digital video. One of the primary IP cores the ODM offers is the SVEN (scalable-video engine), which can handle high-definition, multistandard-compliant video-codec implementations for resolutions as high as 1080i/720p. Supporting SVEN, ODM offers Pictor, an image-processing platform for high-end image processing, and Samba, the first IP for multistandard baseband processing.

PICOCHIP, WWW.PICOCHIP.COM

PicoChip's family of high-performance multicore-DSP devices includes 200 to 300 processors, each a 16-bit Harvard architecture that is programmable with ANSI C, to deliver total performance of 200 GIPS/30 GMACs (billion multiply/accumulates). Although these processors are usable for any high-performance DSP application, the company focuses on the wireless infrastructure. The processor finds use in base stations as a common platform for both WiMax (worldwide interoperability for microwave access) and LTE (long-term evolution). It also supports baseband for femtocells—small base stations for indoor coverage.

PIXELWORKS, WWW.PIXELWORKS.COM

Pixelworks designs, develops, and markets semiconductors and software for the advanced-display industry, including advanced televisions, multimedia projectors, digital-streaming-media devices, and LCD panels. Pixelworks' line of programmable BSPs (broadband-signal processors) can handle multiple codecs for high-quality IPTV (Internet Protocol-television) video and other digital-video applications. The company offers the DreamStream application-reference software for designers using the BSP chips. In addition to the BSP ICs, Pixelworks offers single-purpose discrete ICs and SOCs (systems on chips) that can process and enhance the video signal throughout the entire path in the system.

RC MODULE, WWW.MODULE.RU

The RC (Research Center) Module design center provides IP (intellectual property) for VLIW/SIMD (very-long-instruction-word/single-instruction/multiple-data) processors with a flexible and high-performance vector-matrix engine. The architecture targets industrial video-image processing and navigation and provides scalable performance by employing a programmable operand width of 1 to 64 bits. The NeuroMatrix DSP family includes NM6403/04 chips and synthesizable NMC2 cores.

The new NMC3 core is the next generation of NeuroMatrix-core family with performance that offers an eight-stage pipeline and 8000-instruction cache that supports eight read/write-memory operations per clock cycle and accelerated vector-unit-operand loads. The new NM6405 processor will provide silicon proof for the NMC3. RC Module offers an SOC (system-on-chip)-design service that it bases on NMC3 and ARM's AR-M1176JZF-S core.

RENESAS TECHNOLOGY, WWW.RENESAS.COM

Renesas Technology's SuperH family includes a series of high-performance, 32-bit RISC processors with DSP capabilities. The SH-2A and SH-4A employ a superscalar architecture with a built-in FPU (floating-point unit) for higher performance, delivering as much as 1080 MIPS. The SuperH architecture integrates both DSP and FPU capabilities into one RISC CPU core to save power and overall system cost. These devices are compatible with the previous-generation devices.

RF ENGINES, WWW.RFENGINES.COM

RF Engines cores and SOC (system-on-chip) designs primarily target Xilinx and Altera FPGAs for applications in wireless-communications systems, electronic warfare, spectrum analysis, and medical instrumentation. The HyperLength cores support a 1 million-point transforms running at complex sample rates as high as 200M samples/sec on a Xilinx Virtex II 3000. The Matrix cores include a set of different-length DFT (discrete-Fourier-transform) cores that combine to allow the configuration of an FFT (fast Fourier transform) to

match the number of points an application requires.

The ChannelCore64 can extract as many as 64 narrowband channels from one or two wideband ADC inputs. The PFT (pipelined-frequency-transform) multichannel-filter bank targets use in real-time applications. The Polyphase DFT, or WOLA (weighted overlap and add), is a method of implementing a uniformly distributed multichannel-filter bank. The tunable PFT supports on-the-fly reconfiguration to any frequency plan as a digital front end for the telecommunications, defense, and instrumentation markets. The SpectraChip cores provide a digital replacement for analog intermediate-frequency filtering.

SENSORY, WWW.SENSORYINC.COM

Sensory's RSC (recognition/synthesis/control) family of devices performs recognition, speech synthesis, and general-purpose product control. The RSC line supports speaker-independent recognition, speaker-dependent recognition, speaker verification for voice biometric security, 2400-bps speech compression for speech playback, and music synthesis. The RSC-4x family provides on-chip integration of features, including a microphone preamplifier, twin-DMA units, a vector accelerator, and a hardware multiplier. Sensory's SC-6x series of DSPs offers multiple options for introducing speech- and music-synthesis abilities into consumer products.

SILICON HIVE, WWW.SILICONHIVE.COM

Silicon Hive, a supplier of semiconductor IP (intellectual property), designs, builds, and licenses application-specific products for communications and media processing, tuned processor cores, and program-development tools with application libraries.

The company's processor lineup includes the Avispa-CH1, a high-performance, C-programmable data processor for communications signal processing. The Avispa-IM2 is a general-purpose C-programmable data processor. These two processors are scalable to a high level of operations per cycle, with multiple options for precision, I/O, and memory configurations. The C-programmable SIMD (single-instruction/multiple-data) Moustique-IC2 processor targets image-signal-processing applications with multiple options for SIMD-vector dimension, I/O, and memory configurations.

STMICROELECTRONICS, WWW.STM.COM

STMicroelectronics' portfolio includes application-specific products containing a large proprietary IP (intellectual-property) content and multisegment products that range from discrete devices to high-performance microcontrollers, secure smart-card chips, and MEMS (microelectromechanical-system) devices. Within its portfolio of products, ST develops a family of high-performance VLIW (very-long-instruction-word) cores targeting primarily the consumer, mobile, and computer-and-peripheral market. The ST240 is the latest core offering from the ST200 family of VLIW processors

STREAM PROCESSORS, WWW.STREAMPROCESSORS.COM

Fabless-semiconductor company SPI (Stream Processors Inc) offers parallel-processor options targeting consumer and industrial applications. Its stream-processor architecture reduces computational costs to ASIC levels and makes the performance benefits of parallel processing easily accessible to programmers.

SPI began shipping its Storm-1 family of stream processors in 2006, targeting video and image processing in applications such as intelligent video surveillance, high-definition videoconferencing, broadcasting, and multifunction printers. The Storm-1 family comprises four software-compatible products—from the low-cost, low-power SP8LP-G30 suitable as a single-chip IP (Internet Protocol) camera product, to the SP16HP-G220, which delivers 448 GOPS (billion operations/sec) of computational performance and targets high-end imaging and multichannel video applications. The stream-processor architecture combines data parallelism with a sophisticated C-development environment to simplify programming.

STRETCH, WWW.STRETCHINC.COM

Stretch offers a family of software-configurable processors with embedded programmable logic to target imaging and video, mobile/wireless, security, and industrial applications. Using C/C++ programming tools, system developers can automatically configure Stretch's processors to address changing application needs. Stretch's S6000 family of software-configurable processors targets high-performance video- and wireless-signal processing. The S6 architecture offers a second-generation ISEF (instruction-set-extension fabric), a processor array, and a programmable accelerator.

Stretch and its partners offer reference hardware and software applications for main-profile, standard-definition- and high-definition-resolution MPEG-2 and H.264 video encoding. Stretch and its partners also offer hardware and software applications for WiMax (worldwide-interoperability-for-microwave-access) base-station equipment.

TENSILICA, WWW.TENSILICA.COM

Tensilica offers both Diamond Standard DSP-optimized processor cores and Xtensa configurable processors. The Diamond Standard family includes three DSP-optimized cores. The Diamond three-issue VLIW (very-long-instruction-word) 545CK DSP has eight-way SIMD (single-instruction/multiple-data) units, dual 128-bit load/stores, and a Viterbi convolutional-coder accelerator. The Diamond 330HiFi audio engine includes dedicated audio instructions to decrease frequency requirements and supports more than 30 popular audio encoders and decoders. The Diamond 388VDO video engine targets D1 standard-definition resolution and offers H.264 baseline and main-profile decoding, H.264 baseline profile encoding, and other software for JPEG, MPEG, and VC-1/WMV9. Other Diamond Standard processors, including the 212GP, the 232L and the 570T, incorporate 16-bit MAC (multiply/accumulate)

units, a 32×32-bit multiplier, and integer dividers for easier DSP tasks.

Xtensa processors allow designers to select and configure predefined elements of the architecture and invent instructions and hardware-execution units to maximize performance. The Xtensa LX2 processor core with the Vectra DSP engine supports wide datapaths and traditional DSP tasks. The system can deliver RTL-equivalent I/O through a ports-and-queues mechanism that directly connects to the processor's execution unit to bypass the load/store operation. The Vectra LX DSP engine uses 64-bit instruction words containing three-issue slots for ALU (arithmetic-logic-unit), MAC, and load/store operations.

TEXAS INSTRUMENTS, WWW.TI.COM

Texas Instruments offers a broad portfolio of programmable DSPs. The TMS320C5000 DSP platform targets the consumer digital market and its convergence with communication electronics. With power consumption as low as 0.33 mA/MHz and performance as high as 600 MIPS, C5000 DSPs suit portable media and communication products, including digital-music players, GPS (global-positioning-system) receivers, and portable medical equipment.

The TMS320C6000 DSP platform comprises high-performance fixed- and floating-point DSPs targeting video, imaging, broadband-infrastructure, and performance-audio applications. Running at 350 MHz, the TMS320C6727B DSP is TI's highest performing floating-point DSP. The TMS320C6424 and C6421 DSPs, available for prices starting at $8.95 (10,000), provide performance of as many as 4800 MMACs (million multiply/accumulates) at 600 MHz. The 900-MHz TMS320C6452 DSP targets process-intensive multichannel infrastructure and medical-imaging systems. TI's new 1.2-GHz TMS320C6455 DSP is the company's fastest single-core DSP.

DaVinci technology comprises scalable, programmable processors, software, tools, and support that work together to ease the development of digital-video applications. The TMS320DM647 and DM648 DSPs target multichannel video-security and infrastructure applications and provide a seamless migration path for video-processing applications based on the TMS320DM642. The TMS320DM355 digital-media processor aims at portable, high-definition video products and comprises an integrated video-processing subsystem, an MJCP (MPEG-4-JPEG coprocessor), an ARM926EJ-S core, and peripherals. TI's newest DaVinci processor, the TMS320DM6467, is a single-chip, real-time HD (high-definition)-video-transcoding option that allows consumers to seamlessly move content across their video end products, such as media gateways, multipoint-control units, digital-media adapters, video-security DVRs (digital-video recorders), and IP (Internet Protocol) set-top boxes.

The TMS320C2000 DSC (digital-signal controller) combines control-peripheral integration and ease of use with the processing power and C-language efficiency of TI's DSP technology. TI's new TMS320F2833x controller series comprises floating-point DSCs that provide 300-MFLOPS performance at 150 MHz and enable energy-efficient industrial applications.

To address the market need for advanced yet easy access to information and media, TI's OMAP (Open Multimedia Applications Platform), including OMAP3503, OMAP3515, OMAP3525, and OMAP3530, provides the best general-purpose, multimedia, and graphics processing. The ARM Cortex-A8 core provides laptop-like performance at handheld-system power levels. TI's scalable OMAP processors provide a variety of combination options, including the Cortex-A8 core, multimedia-rich peripheral, accelerators, and TMS320C64x+ DSP core to address demand for increased graphics and Web-browsing capabilities.

TI's TMS320TCI6488 integrated multicore-baseband processor targeting W-CDMA (wideband-code-division-multiple-access) wireless infrastructure basestations. The 3-GHz-TCI6488 supports the necessary baseband functions for a macro base station on a single chip. The TCI6488 can support both voice and data transmission with low latency, including 48 users per device in an HDSPA (high-speed-downlink-packet-access)-macro base station.

The 65-nm, single-core, 1-GHz TMS320TCI6484 DSP combines both MAC

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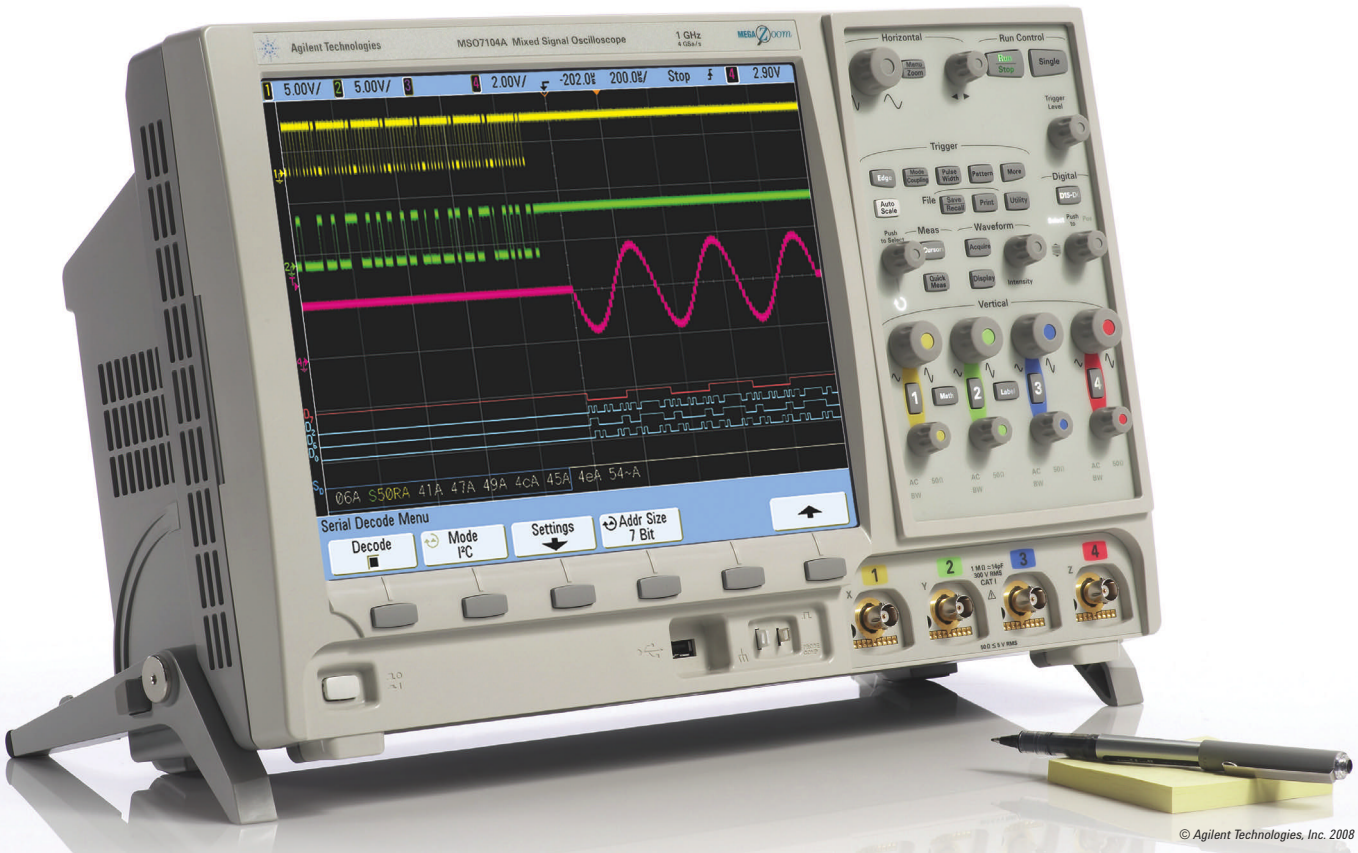

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Agilent Technologies

(media-aqccess-control)- and PHY (physical)-layer functions on one chip to support multiprocessing beyond 3G cellular-infrastructure applications, including HSPA/HSPA+, LTE (long-term evolution), and WiMax (worldwide interoperability for microwave access) Wave 2. Based on TI's TMS320C64x+ core, the TCI6484 DSP supports symbol-rate processing at 34 Mbps, reduces latency for better quality of service, and eliminates the need for a RISC coprocessor. The MAC/PHY-layer functions make the TCI6484 a scalable, converged option that is reusable across pico, micro, and macro base stations.

NEW TILERA, WWW.TILERA.COM

Tilera offers high-performance multicore processors targeting embedded networking, security, multimedia-processing, and wireless-infrastructure applications. The Tile processor family targets applications requiring intensive packet processing for layers 3 through 7 at 1- to 20-Gbps throughput. Services such as deep packet inspection, flow monitoring, and intrusion prevention are ideal targets for Tilera's processors. In the multimedia and DSP arena, the Tile processors enable HD (high-definition)-video applications, such as videoconferencing, surveillance, and broadcast head-end equipment, as well as wireless backhaul and baseband processing.

The Tile64 processor SOC (system on chip) has 64 full-featured processor cores plus system-integration blocks, including four DDR2-memory controllers with ECC (error-correcting code); two 10-Gbps, four-lane PCIe (Peripheral Component Interconnect Express) interfaces; two XAUI (10-Gbit-attachment-unit-interface) 10-GbE (Gigabit Ethernet) controllers, two 1-Gbit RGMII (reduced-Gigabit media-independent-interface) Ethernet controllers; and 64-bits of flexible I/O that can support HD-video input or other high-speed interfaces. The device includes 5 Mbytes of cache, and each processor core can independently run a full operating system, such as Linux. It is available in speeds of 600 to 866 MHz.

Tilera based the Tile64 family on a tiled, multicore architecture with a mesh-based on-chip interconnect that delivers as much as 32 Tbps of interconnect bandwidth between the cores and allows scaling the architecture beyond hundreds of cores.

NEW VERISILICON, WWW.VERISILICON.COM

The VeriSilicon IC-design foundry provides custom and SOC (system-on-chip) turnkey services. The company last year acquired the ZSP division of LSI Logic. VeriSilicon's licensable ZSP DSP and IP (intellectual-property)-based SOC platforms target application markets for voice and wireless communications and multimedia.

XILINX, WWW.XILINX.COM

Xilinx offers PLDs and FPGAs. Its XtremeDSP includes a portfolio of DSP devices that target high-performance signal processing with software tools that support design development in Matlab, Simulink, and C/C++, along with development kits and reference designs in wireless and video applications. Xilinx XtremeDSP application-optimized products are also available for medical imaging, military/aerospace, mobile/wireless-base-station, imaging, and video systems.

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CTLSH1-40M832D	1.0	40	Dual, Schottky	3 x 2 x 0.9	TLM832D
CTLSH2-40M832	2.0	40	Single, Schottky	3 x 2 x 0.9	TLM832
CTLSH3-30M833	3.0	30	Single, Schottky	3 x 3 x 0.9	TLM833
CTLSH5-40M833	5.0	40	Single, Schottky	3 x 3 x 0.9	TLM833

Transistors

Central Type No.	I_C (A)	V_{CBO} (V)	Description	TLM Size L x W x H (mm)	Package
*CTLT3410-M621	1.0	40	Low $V_{CE(SAT)}$, NPN	2 x 1 x 0.8	TLM621
*CTLT7410-M621	1.0	40	Low $V_{CE(SAT)}$, PNP	2 x 1 x 0.8	TLM621
CTLT853-M833	6.0	200	High Current, NPN	3 x 3 x 0.9	TLM833
CTLT953-M833	5.0	140	High Current, PNP	3 x 3 x 0.9	TLM833

Combo: Low $V_{CE(SAT)}$ Transistor and Low V_F Schottky Rectifier MDM

Central Type No.	Transistor		Rectifier		TLM Size L x W x H (mm)	Package
	I_C (A)	V_{CBO} (V)	I_F (A)	V_{RRM} (V)		
CTLM1034-M832D (NPN)	1.0	40	1.0	40	3 x 2 x 0.8	TLM832D
CTLM1074-M832D (PNP)	1.0	40	1.0	40	3 x 2 x 0.8	TLM832D

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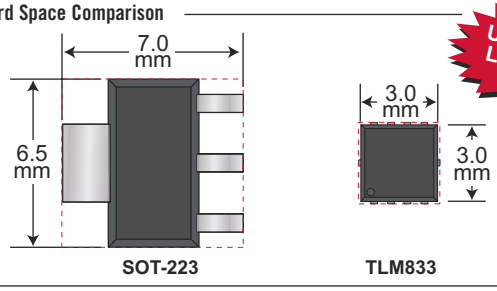

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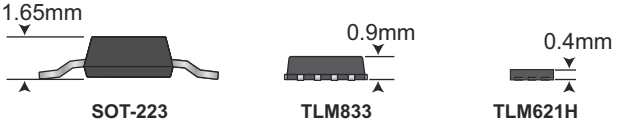

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BY NEERAJ KAUL AND STEVE KISTER • SYNOPSYS INC

Using IC prototyping to optimize design implementation

MAKING THE RIGHT TRADE-OFFS DURING IC PROTOTYPING CAN MINIMIZE RISK AND ULTIMATELY SAVE TIME AND MONEY.

As IC-design size continues to escalate, time-to-market windows tighten, design requirements become more stringent, and device geometries shrink to nanometer proportions. Because of these constraints, employing prototyping early in the design cycle is gaining in significance. Problems lurk within these increasingly complex ICs. These problems can kill a project if you find them too late in the design cycle. Although IC prototyping solves these problems, there are as many definitions of this approach as there are techniques for its execution. This article focuses on defining prototyping for modern designs, including key requirements and useful techniques for putting prototyping into practice.

It can be costly to learn late in the design cycle that a design cannot meet your specifications. At a minimum, the schedule will slip, necessitating additional engineering time and lengthening time to market. The worst possible outcome is a canceled project, forfeiting months of work from many groups and missing the market window. IC prototyping addresses these risks. IC prototyping is similar to physical implementation in that it includes placement, routing, and optimization. However, its objective is to determine the feasibility of implementing a design within the given specifications. Early in the development cycle, a wide range of possible implementation approaches is available. Prototyping allows design teams to confirm that a chosen approach is viable. By finding potentially fatal problems early in the development process, design teams and managers can assess changing design specifications and make the architectural, functional, and die-size changes necessary to save the project from an untimely death.

Chip-design specifications fall into the primary categories of functional, timing, power, and area. The functional category defines what the design is supposed to do. The timing category describes how quickly the design should perform its functions, including such specifications as clock-cycle times. The power category defines how much power a chip can consume while in various operating states, from idle through any number of functional states. Area defines the size of the chip, which relates to cost; larger chips cost more to produce. Physical implementation directly affects area, timing, and power. If a design team cannot meet one or more of these specifications,

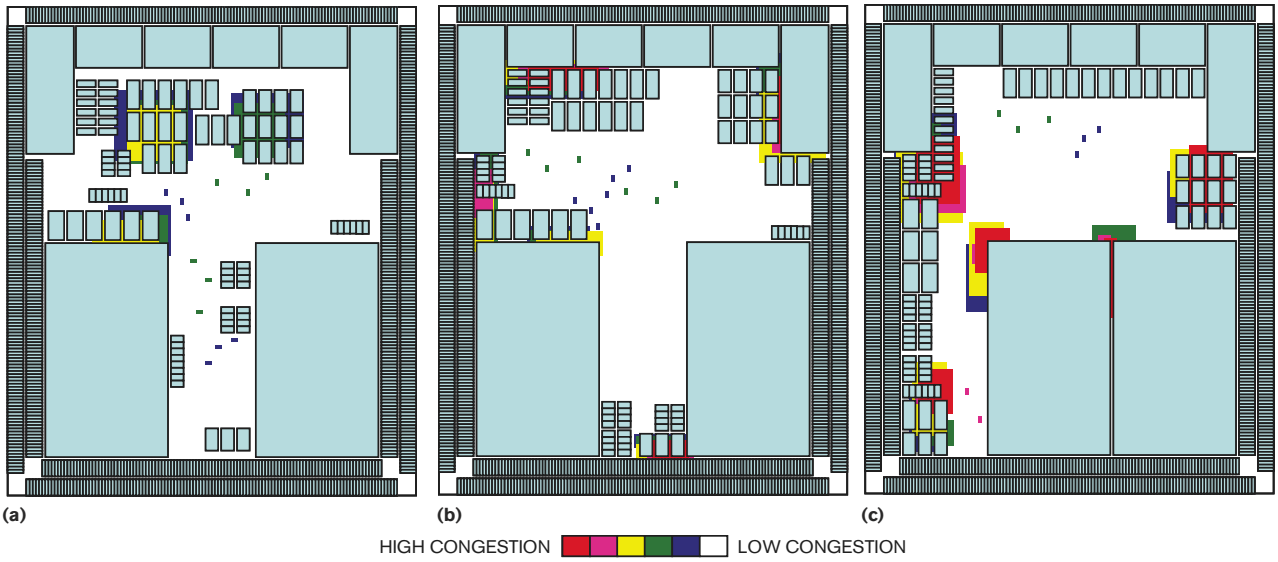

Figure 1 The congestion maps for three scripted-prototyping runs show a good implementation strategy (a), a slightly worse one (b), and a poor one (c).

the team must modify the physical or logical implementation or even the overall function of the design.

The key to IC prototyping is doing enough to find gross problems without expending the time and effort to perform the full implementation. Designers have a finite amount of time to complete a design and, therefore, limited time for prototyping. Moreover, designers can take many approaches to design implementation. Faster placement, routing, optimization, and analysis during prototyping permit designers to quickly explore many implementation strategies. This article describes the key process requirements for prototyping, as well as its objectives and benefits for netlist and constraint handling, placement, power and signal routing, and analysis.

PROTOTYPING-PROCESS REQUIREMENTS

A successful IC-prototyping strategy is one that designers can complete quickly so that they can assess the feasibility of the design as early in the development cycle as possible. This strategy requires designers to start working early with design data, which may be incomplete or inaccurate. Thus, prototyping tools must tolerate this data and help designers identify problems with the data. Proving feasibility does not mean completing an error-free implementation. Rather, prototyping shows designers the number and difficulty of the problems they will face during detailed implementation.

How much time you allocate to IC prototyping depends on your overall schedule. If the design-implementation schedule requires a few weeks, prototyping should take no more than a few days. If implementation requires several months, prototyping should take just weeks. To minimize the time to complete prototyping, designers must make trade-offs between completeness and accuracy. These trade-offs necessitate the use of analysis tools to monitor the predictability of the prototype.

Support for scripting is also important. Creating trial layouts should take minimal time to allow engineers to focus on analyzing results and determining next steps. An efficient IC-prototyping process enables designers to quickly generate multiple trial layouts. Using this analysis, designers work with one or more of the trial layouts or generate additional layouts. Once a trial layout shows promise, designers can quickly make incremental updates and perform what-if analysis.

Table 1 and **Figure 1** illustrate the results of a scripted-prototyping approach. One run of the prototyping script creates several floorplans for the design. The script also produces the HTML (hypertext-markup-language) table. Each row of the table is for one floorplan of the design. The table makes it easy for the user to see which floorplan is the best and whether any of the floorplans should become the basis for the final floorplan of the design. The **figure** also shows routing-congestion maps for three of the floorplans. The maps clearly indicate that the floorplan gets progressively worse (**Figure 1a** and **1b**) as an implementation strategy, and the map in **Figure 1c** should not become the basis for the final floorplan.

EARLY NETLIST AND CONSTRAINT HANDLING

In IC prototyping, designers start with design data that they acquire early in the process. This data likely has errors, such as missing library components; netlists referencing pins on non-

TABLE 1 SCRIPTED-PROTOTYPING RESULTS

		Setup time (nsec)				Virtual in-place-optimization setup time		Congestion*			Links
Run	Objective	Worst negative slack	No. of violating paths	Sum of negative slack of all violating timing paths	Timing	Worst negative slack	Sum of negative slack of all violating timing paths	Total	Maximum/ percentage	Wire length (microns)	Place-and-route summary report/run
No.	Hierarchical gravity/timing driven	−21.54	5048	−10,596	Report	−2.25	−1588	21,767	29/0.2	56,447,834	Place and route/log file
1	Hierarchical gravity	−19.56	4078	−5886	Report	−2.1	−1412	21,831	28/0.2	56,453,440	Place and route/log file
2	Hierarchical gravity/macros on edge	−21.27	5476	−18,410	Report	−3.07	−1980	85,565	102/ 0.3	76,652,906	Place and route/log file
3	Congestion	−19.98	4879	−6812	Report	−2.06	−1324	28,422	113/0.2	55,214,522	Place and route/log file
4	Hierarchical gravity/ congestion driven/timing driven	−27.08	4368	−12,559	Report	−2.14	−1247	87,588	144/0.3	62,468,571	Place and route/log file
5	Grouping/ macros on edge	−40.07	8742	−37,612	Report	−2.66	−2117	435,761	859/1.6	108,781,409	Place and route/log file

*Map

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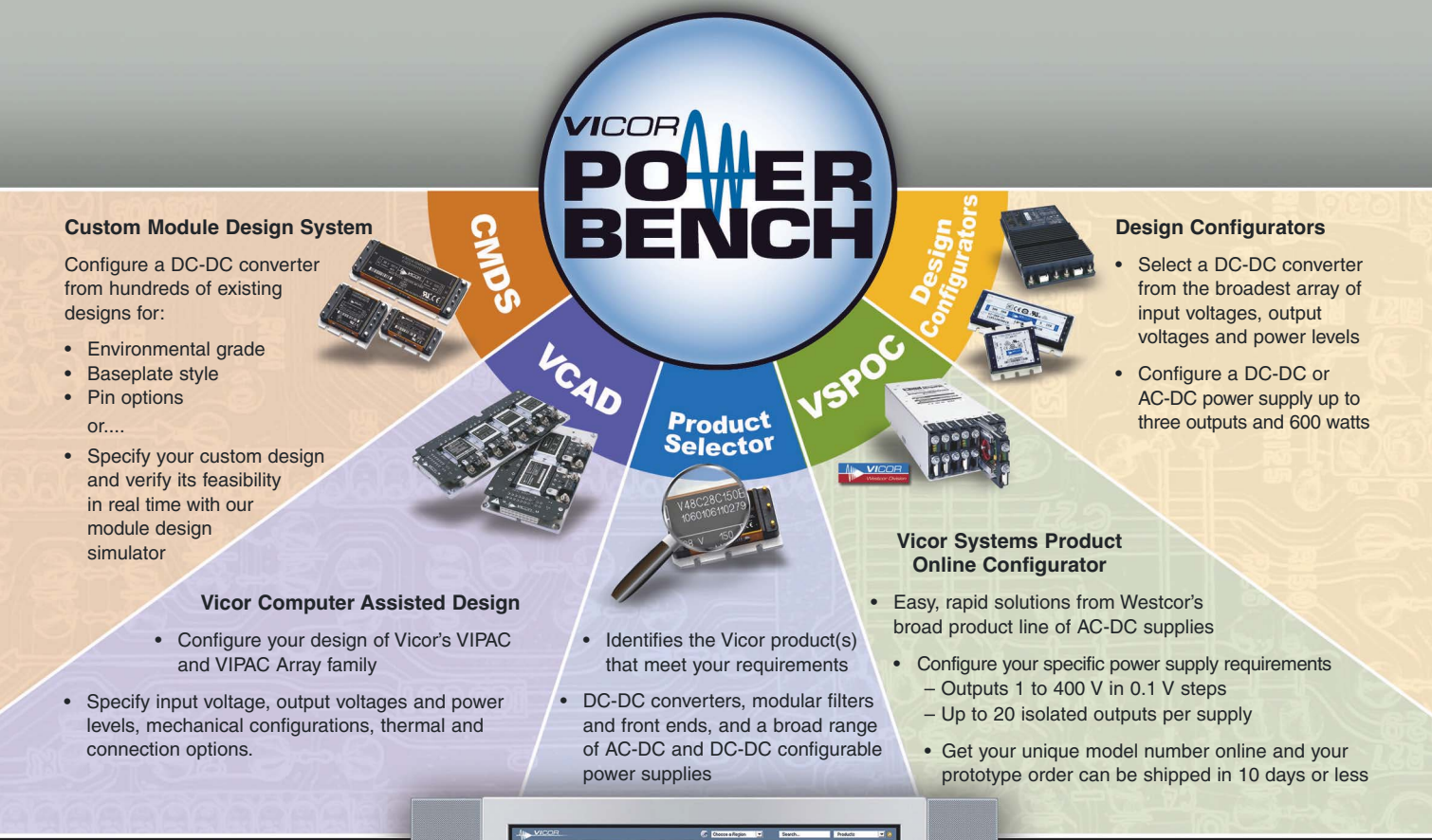

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existent cells; and timing constraints that reference nonexistent starting points, endpoints, or even clocks. To complete detailed physical implementation, designers must resolve these errors before continuing with the design. Prototyping allows designers to proceed with the design even during the detection and reporting of errors. Designers can handle missing components as black boxes, ignore extra cell pins, and omit the application of timing constraints. Reporting is important because it allows designers to assess both the type and the quantity of the errors. The prototyping tool can also provide utilities to help the designer temporarily correct errors associated with the bad data.

Starting physical prototyping at the RTL (register-transfer level) or with RTL data that you do not map to a real gate-level netlist is problematic. The most common risk factors with these netlists are that they do not accurately reflect the size of the final netlist and that their lack of gates makes the prediction of congestion dubious. Results may appear to achieve timing closure, but, when you map the results to physical gates, the timing differs. The best approach for physical prototyping is to use the available netlist with the highest quality input—ideally, one you generate using the target physical-cell library to enable physical placement and routing. Some synthesis tools require the use of statistical or custom wire-load models to estimate interconnect loading, whereas others can read information from physical-cell libraries to more accurately predict area and interconnect loading on a design-by-design basis. This approach enables accurate assessment of an implementation strategy's feasibility.

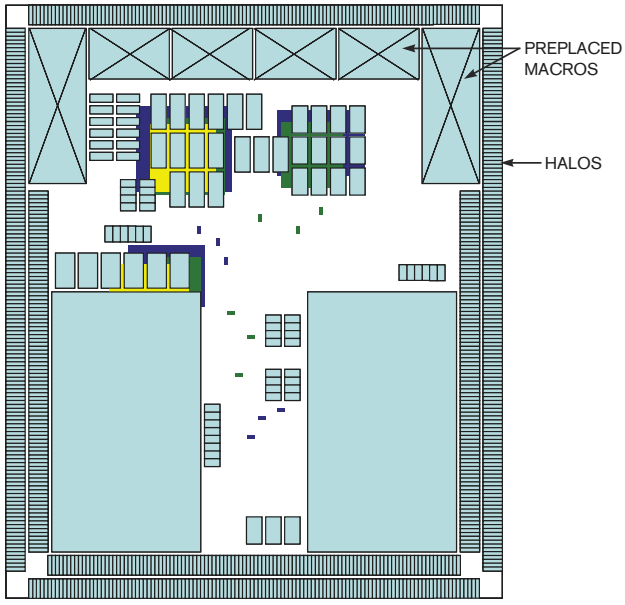

Figure 2 You can add halos to macros with congestion near the macros' edges. The two large macros (top left and top right) are good candidates for fixing in position before performing more trial runs.

PROTOTYPE PLACEMENT

The primary objectives of IC-prototype placement are to determine the best placement of the principal floorplan elements, such as I/Os, pins, and hard and soft blocks, and to quickly provide an estimate of the design's performance that you base on this floorplan. Today's designs typically have tens or hundreds of hard macros. Although they vary greatly in size, all hard macros represent routing obstructions that can create routing congestion. Given these constraints, prototype-placement algorithms must automatically and simultaneously handle hard macros and standard cells, considering routing congestion, timing, and voltage domains. Initially, designers manually place and fix the locations of critical macros and then assess the routing congestion and timing of multiple placement approaches. Some hard-macro placements work well, whereas others require refinement. The placement tools must accommodate incremental placement of the remaining

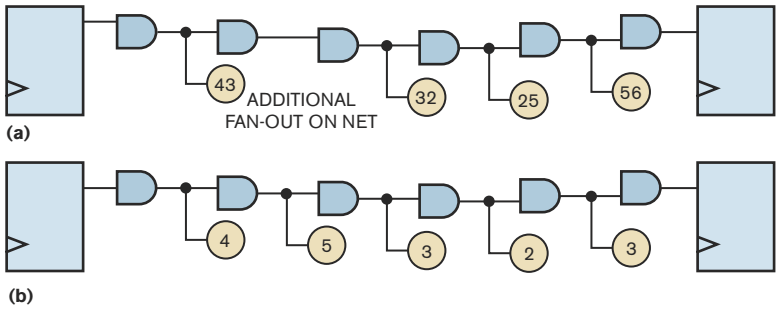

Figure 3 These paths have the same value of negative slack. Large fan-outs contribute to a significant amount of delay (a). You can easily fix it by buffering to reduce the nets. Small fan-out nets do not contribute to significant delay (b).

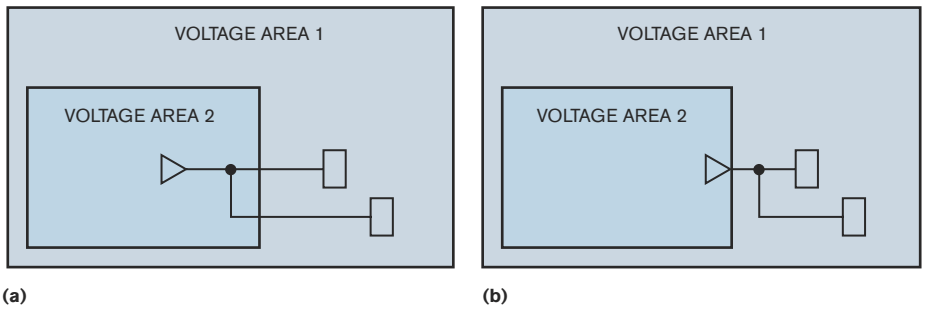

Figure 4 The output of the level shifter in Voltage Area 2 must drive long wires that cross Voltage Area 2 (a). Buffers can help only if you place them in Voltage Area 1. Placing a level shifter near the edge allows you to add buffers close to the level-shifter output and simplifies the power connections to the level shifter (b).

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macros, rather than require designers to do over the placement from scratch.

In the early stages of IC prototyping, the channels between hard macros often contain congestion, due both to the macros' being too close to each other and to the presence of standard cells in the channels. You can prevent these phenomena from occurring by using IC-prototype-placement tools that support hard-macro "halos" that reserve space for routing connections surrounding the edges of the block. If the placer cannot honor halos, the designer must manually move the hard macros and add placement blockages within the channels. A few iterations may be necessary before you arrive at the appropriate channel sizes. **Figure 2** provides an example of the information designers can see in an IC prototype to help guide refinement of an implementation strategy.

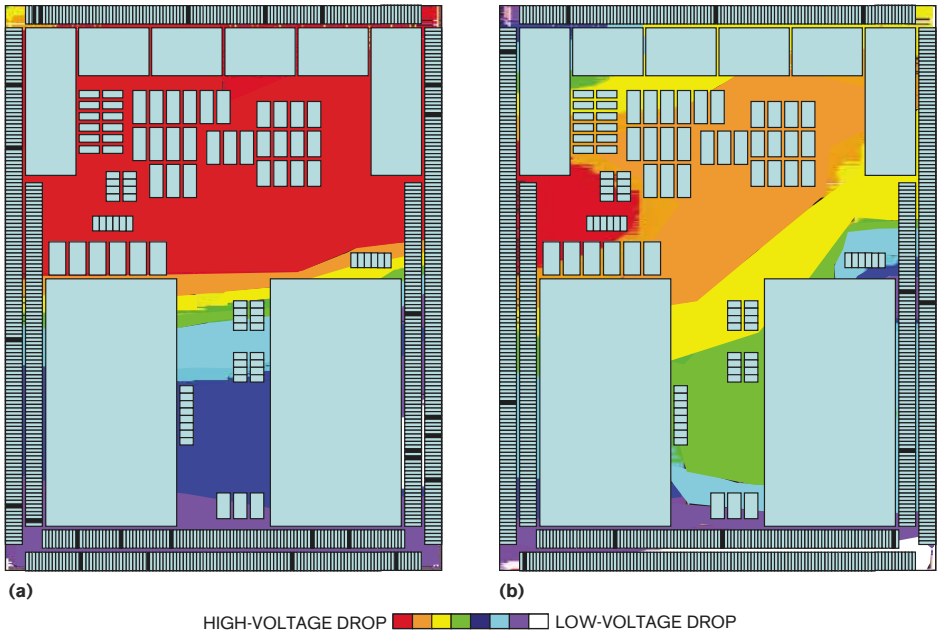

Figure 5 Placing power pads in groups or in poor locations produces poor voltage-drop characteristics (a). A design with fewer power pads (black) has better voltage-drop characteristics (b).

Netlists you develop early in the design cycle often have many high-fan-out nets; some, such as clocks, are timing-critical, and others, such as asynchronous-reset nets, are not. Physical-layout designers typically optimize these nets during detailed implementation. Prototype-placement algorithms

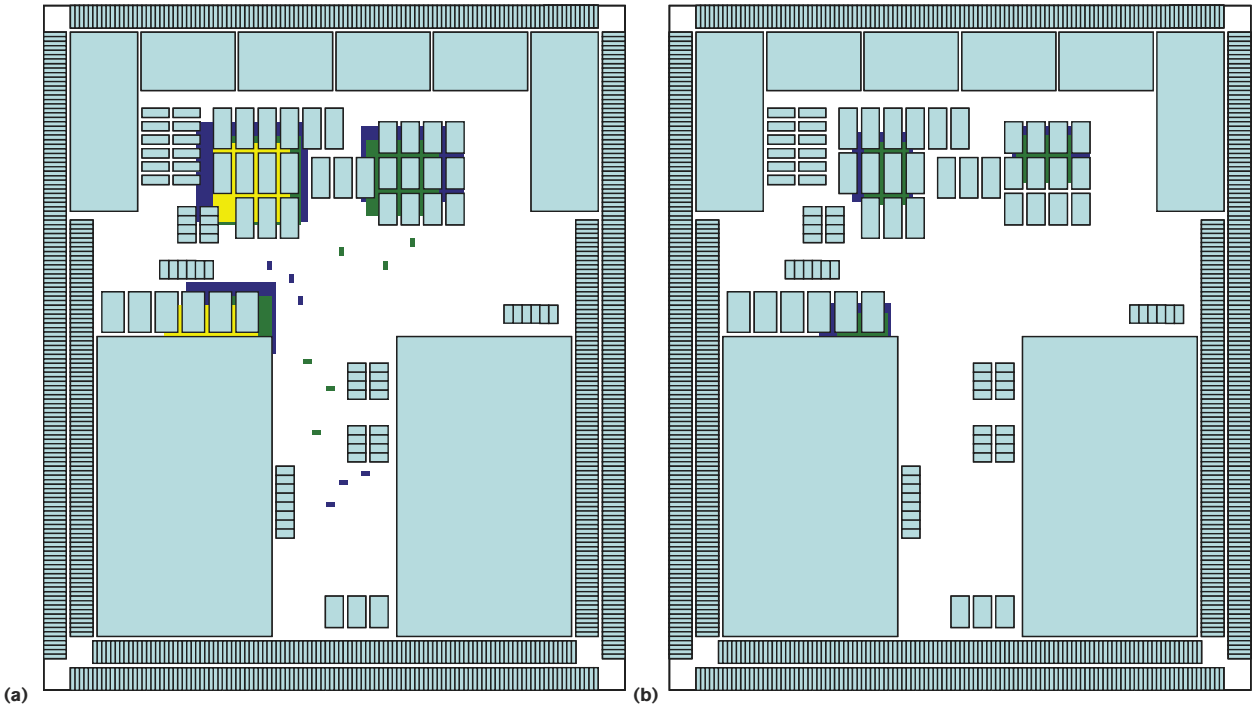

Figure 6 The congestion maps of the same design show more congestion (a) and less congestion (b). The prototype router spends less effort to remove congestion than the implementation global router does. The designer can adjust the floorplan to reduce congestion. Thus, detailed implementation routing is more likely to complete without problems.

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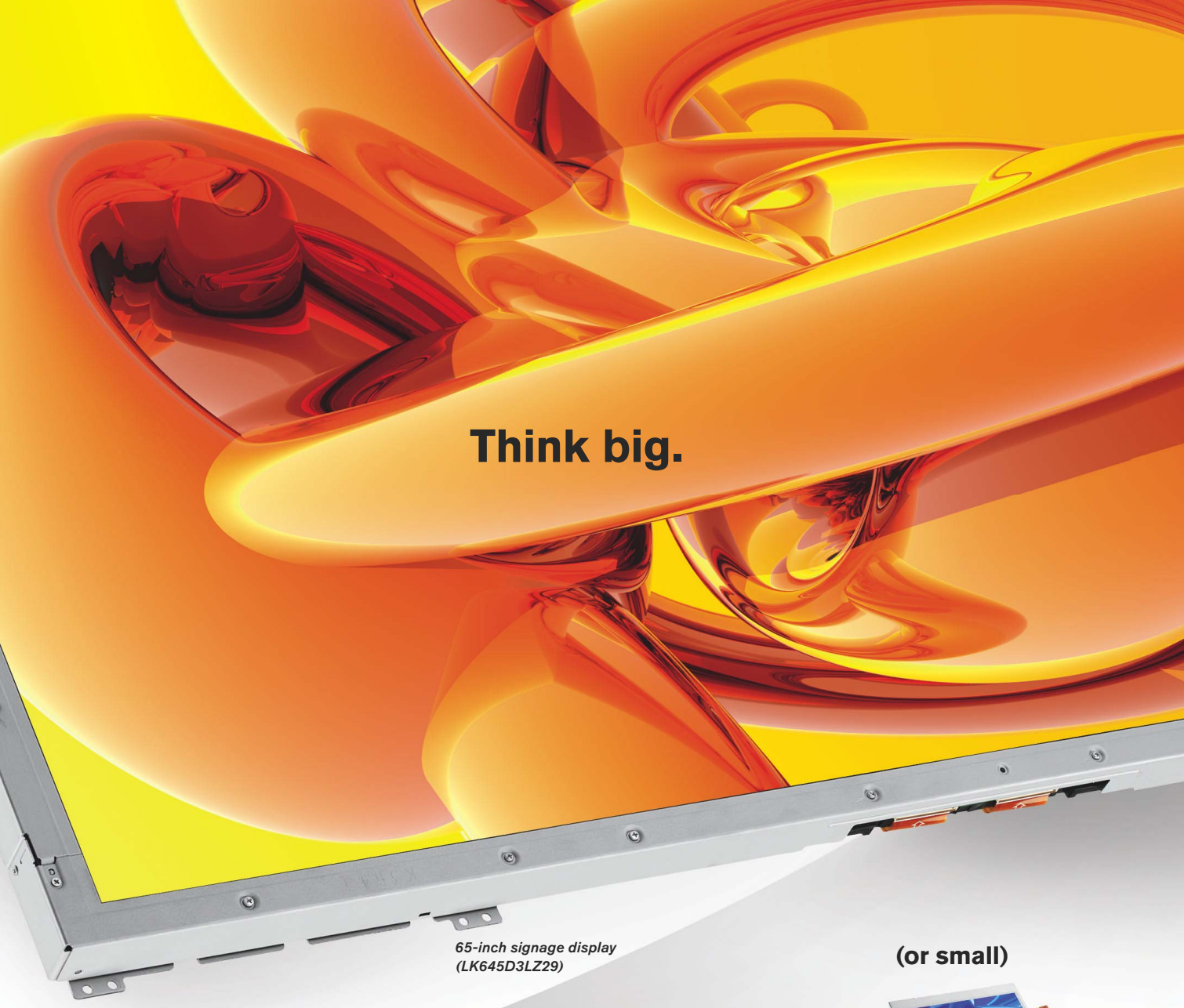

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should ignore these types of nets. If they cannot, the standard-cell logic is likely to create unnecessary congestion. Moreover, netlists you develop early in the cycle pose a problem for timing-driven placement algorithms. The netlists often contain many violating timing paths; fixing these violating paths can sometimes be difficult. Most timing-driven placement algorithms place equal weight on both those paths that are difficult to fix and those paths that are easy to fix, making it difficult to distinguish between them.

One approach to these problems, albeit time-consuming—and, hence, costly—is first to run placement focusing on alleviating congestion, next to perform in-place optimization, and then to run timing-driven placement. A more elegant approach is to use a placement engine that can execute virtual optimization on the input netlist, eliminating all but the toughest of violating timing paths. This approach produces a placement scheme that you accomplish by optimizing the hard-to-fix paths. **Figure 3** compares an easily fixed timing path with a more challenging one.

Many of today's designs have multiple voltage domains within the core area. To accommodate the logic that connects to a voltage domain, a designer must create voltage areas within the core area. But what is the best location for these voltage areas, and how large should they be? Prototype-placement algorithms must be aware of voltage domains and assemble logic that connects to one domain. The results allow designers to quickly define the size and location of voltage areas within the chip.

If the placement algorithm is unaware of voltage domains, the designer must predefine voltage areas before placement using regions and then assign logic for each voltage domain to its region. This approach forces designers to place voltage domains in the predefined regions. As a result, designers must iterate through a number of placement runs to refine the region sizes.

Multiple voltage domains also require level shifters, which are placed on nets that connect one voltage domain to another. Designers place notoriously slow level shifters at the edges of voltage areas to optimize timing (**Figure 4**). Prototype-placement algorithms must be able to recognize and appropriately place level shifters. Again, an alternative, less-than-ideal approach is to use regions. This approach requires the designer to analyze the interface nets, create regions along edges of voltage areas, and then assign the various level-shifter instances to the appropriate regions.

For large designs, logic designers commonly complete RTL coding and synthesis of some blocks before others. The nonsynthesized blocks are black boxes, because the designer knows nothing but the boxes' interface. IC prototyping supports the placement of black-box shapes, allowing the shape to vary but maintaining enough internal area for the expected "child" cells, once the designer synthesizes them.

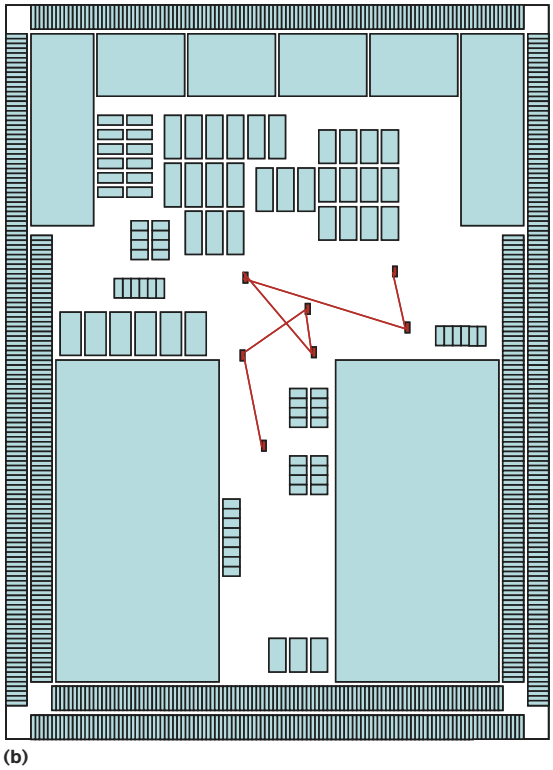
A placement tool can allow virtually flat placement of available cells during the placement and shaping of the black boxes. This approach enables block designers to proceed with the design in parallel with the development of the contents of the black boxes. An alternative strategy is to create dummy hard macros for the nonsynthesized blocks. The designer sets the size and shape of the macros and the layers and locations of pins. The trade-off in this case is that the approach forces the rest of the cell placement to work with the predefined black boxes.

PROTOTYPE-POWER ROUTING

A design's power network consumes routing resources that you could otherwise use for signal routing. IC-prototype power-network generation and analysis should rapidly generate a placeholder power mesh to accurately account for routing resources that the network consumes. This generation and analysis should also create a power network for the design that meets—but does not exceed—voltage-drop and electromigration requirements. You need to know which metal layers you should use for the power routing, how wide the wires should be, and what the distance between power-routing segments should be. Designers often rely on rule-of-thumb guidelines from power-design gurus to form the power mesh, resulting in an overdesigned mesh; that is, it easily meets requirements but at the expense of consuming excessive amounts of routing

Start-Point Name	EndPoint Name
pratichi/cnt_instrn_reg_31/CLK	isha/STACKFSM_in_reg_2_2/DO
pratichi/cnt_instrn_reg_31/CLK	isha/STACKFSM_in_reg_2_7/DO
prem/Oprnd_A_reg_2_6/CLK	prem/Zro_Flag_reg2/D0
prem/Oprnd_A_reg_2_6/CLK	prem/Zro_Flag_reg5/D0
isha/STACKFSM_ot_reg_5/CLK	isha/STACKFSM_obf_reg_1_7/DO
isha/STACKFSM_ot_reg_5/CLK	isha/STACKFSM_obf_reg_1_9/DO
isha/STACKFSM_ot_reg_5/CLK	isha/STACKFSM_obf_reg_1_3/DO

(a)



(b)

Figure 7 Cross-probing from a list of violating timing paths (a) allows designers to see the topology of the path in the prototype layout (b).

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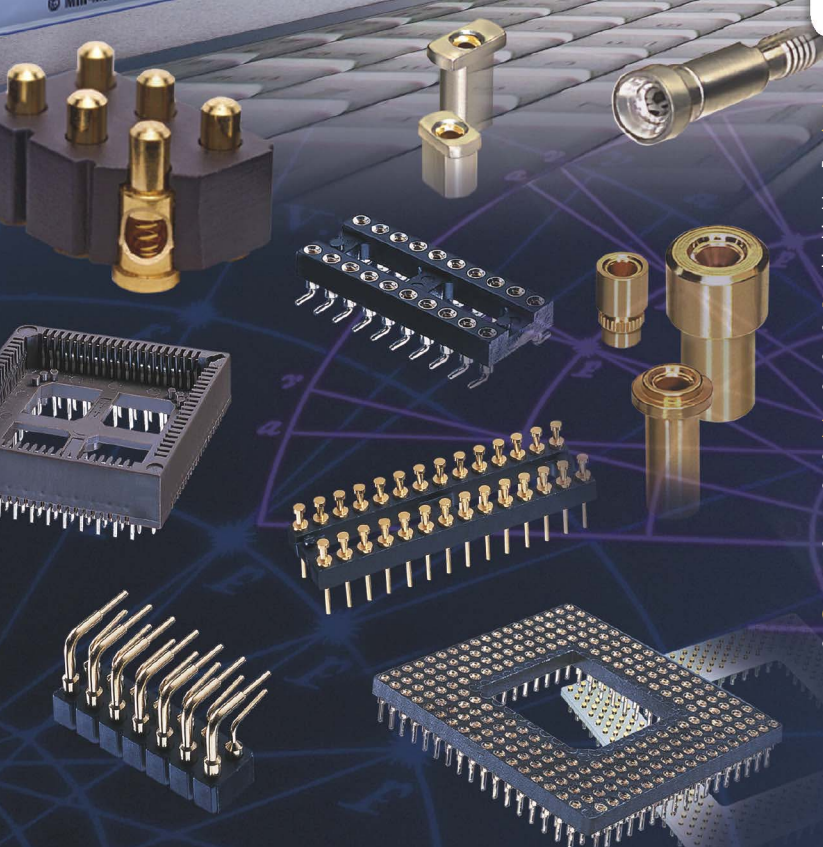

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resources. Using a prototyping-power-network generator enables designers to build efficient power structures.

Some power-implementation tools require that power meshes be physically correct before designers can analyze the voltage drop. For large designs with many cells and many hard macros, this requirement means days of work to prepare the power routing for analysis. This process is not conducive to quick prototyping. A faster approach is to employ a power-network-generation and -analysis tool that can infer connections based on proximity, allowing designers to route the primary mesh structures without performing detailed connections. This approach enables designers to review voltage-drop and electromigration characteristics earlier in the design cycle and even to analyze trade-offs of varying layers, widths, and pitches within the power mesh.

In addition to analyzing various mesh structures during prototyping, it is useful to analyze the voltage-drop and electromigration characteristics of a mesh with varying numbers and locations of power-supply-pad cells. Simply adding supply pads does not always produce improvements. For example, a supply pad behind a hard macro does not easily connect to the mesh and, therefore, cannot deliver a significant amount of current. Prototype-power planning should enable fast what-if analysis of supply-cell placements rather than require the designer to perform detailed connects. The what-if analysis may prove that fewer supply-pad cells are necessary than rules of thumb would predict. Using fewer supply cells produces smaller chips in pad-limited designs (**Figure 5**).

PROTOTYPE-SIGNAL ROUTING

IC-prototype-signal routing's primary objectives are to identify highly congested areas to assess the difficulty of routing an implementation strategy and to accurately predict detailed implementation routing to provide interconnect loading for early timing analysis. Macro placement and power structures often contribute to routing congestion during implementation. Given enough time, routing algorithms of implementation tools perform hundreds of passes in an attempt to route congested areas. During prototyping, it is useful to see the congestion to determine whether changes in the implementation strategy can eliminate the congestion. Reducing or eliminating congestion reduces the effort of completing routing, which, in turn, minimizes the risk of failure to route. IC-prototype routing quickly identifies congested areas and minimizes difficult routing problems (**Figure 6**). Once you minimize congestion, prototype routing should accurately reflect implementation routing, enabling accurate extraction of interconnect loading for use in performing timing analysis on the implementation strategy.

PROTOTYPE ANALYSIS

IC-prototyping tools should provide a comprehensive set of analysis functions that allows designers to identify and as-

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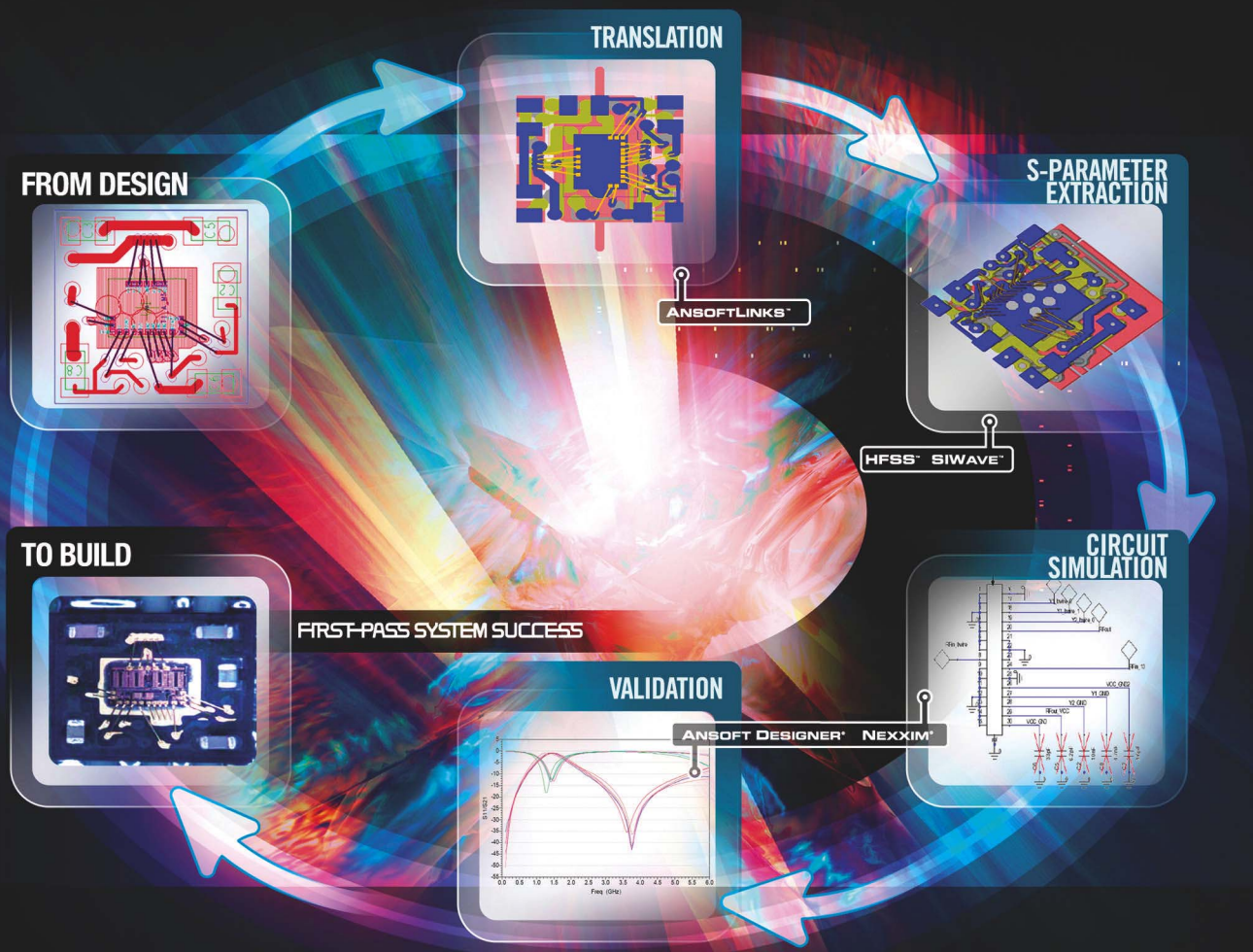

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sess data, routing, timing, and power-consumption problems. These analysis functions also provide a key means for physical-layout designers to communicate with front-end designers. Prototyping-analysis functions should find problems in the input data; quickly identify the big problems related to routing, timing, and power requirements; and facilitate communication between physical-layout and logic designers. The adage "a picture is worth a thousand words" certainly applies to analysis of a physical prototype. A comprehensive set of reporting functions couples with a rich set of visualizations to simplify and speed analysis.

Consider timing analysis. A timing analyzer for IC prototyping highlights major timing problems without requiring the user to run detailed optimization. It accomplishes this task by incorporating virtual optimization into the timer so that the report omits easily fixed timing paths. If you then enable cross-probing from the report to a layout view, you can quickly see the topology of the difficult-to-fix timing paths. This approach also facilitates communication between physical and logical designers. Viewing the report in addition to the path layouts helps logic designers identify missed, multicycle-path, or false-path definitions (**Figure 7**).

Although IC prototyping's objectives differ appreciably from those of detailed implementation, the two approaches have similar steps. Prototyping finds potentially fatal problems early in the development cycle. If prototyping steps complete quickly, designers can assess many potential implementation strategies in the time available for prototyping. To minimize the time to complete the prototyping steps, physical designers and tools must trade off levels of completeness but maintain enough accuracy to reliably find potentially fatal problems. The payoff is a streamlined implementation process, enabling faster design cycles and speedier time to market. EDN

AUTHORS' BIOGRAPHIES

Neeraj Kaul is an R&D-group director at Synopsys Inc (Mountain View, CA), where he has worked for more than eight years. He is responsible for design planning, feasibility, and high-capacity-design methodology. He received a master's degree and a doctorate in electrical and computer engineering in 1992 from Vanderbilt University (Nashville, TN) and a bachelor's degree in technical, electrical, and computer engineering from the Indian Institute of Technology in 1986. Kaul's focus in the EDA industry is timing analysis and optimization, simulation, statistical timing, and physical design.

Steve Kister is a technical-marketing manager at Synopsys (Mountain View, CA), where he has worked for 12 years, focusing on design planning. Kister joined Synopsys in 1995 and has been in the electronics industry for 27 years. He received a bachelor's degree in electrical-engineering technology from DeVry Institute of Technology (Phoenix) in 1979. His experience includes test engineering, physical design, library development, and applications engineering.

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Trip points for IC-timing analysis

GET THE MOST OUT OF YOUR TIMING METHODOLOGY.

If you are a budding timing-analysis engineer or even a veteran, understanding trip points, which all major timing-analysis tools incorporate, is essential. Engineers use trip points in timing-analysis tools to calculate delay and transition values on the various nodes of a design. Timing-analysis engineers must become familiar with the proper use of trip points, as there are many nuances to using them. If engineers overlook them, these nuances can cause problems late in the SOC (system-on-chip)-design cycle, when they need to address timing. A quick tutorial and a bit of timing tool-script work can make their job easier.

DEFINING AND DETERMINING TRIP POINTS

A trip point is the percentage of logic-high levels engineers use a as reference to measure slew and delay values. **Figure 1a** illustrates the slew trip points, and **Figure 1b** illustrates delay trip points.

Engineers use trip points to characterize the delay and transition values of the pins of a standard-cell or hard-block-IP (intellectual property), when checking the timing of an SOC. Typically, engineers can find trip-point values in the timing models, most commonly in Liberty (.lib format). Timing-analysis tools in turn use these values to calculate delays and slews.

Engineers set trip points for a particular technology node while characterizing the libraries for standard cells or hard-IP blocks. The aim of setting a trip point is to ensure that the measured delays and slews are closer to actual Spice waveforms. As **Figure 2** shows, slew values are more accurate when a trip point lies in the linear region of 20 to 80% of the switching waveform than when it lies in the nonlinear region of 10 to 90%. Typically, cell delays that timing tools calculate are closer to Spice results when transition trip points are in the linear region.

Also, the threshold-voltage characteristic for transistors plays an important role in determining a trip point, because the output waveform linearizes after the input voltage crosses the threshold-voltage value for the transistor (**Reference 1**).

Delay thresholds are fixed in the linear region of the input and output waveforms. It does not matter whether the delay trip points are in the 20 to 80% region or at 50%, as long as they lie in the linear part of the waveform. **Listing 1**, which is available at www.edn.com/ms4272, is a snapshot of a typical timing model (in .lib) to indicate the trip points under use.

TIMING TOOLS CALCULATE DELAYS

Timing tools calculate delays using trip points in many ways. When both the driver and the load have the same delay

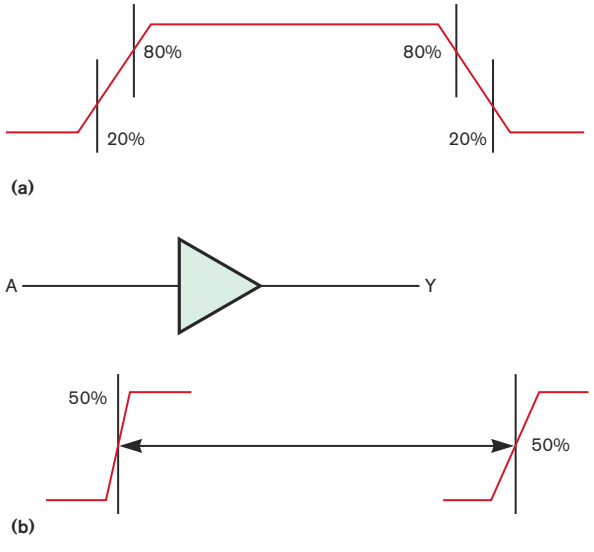

Figure 1 A trip point is the percentage of logic-high levels engineers use a as reference to measure slew (a) and delay (b) values.

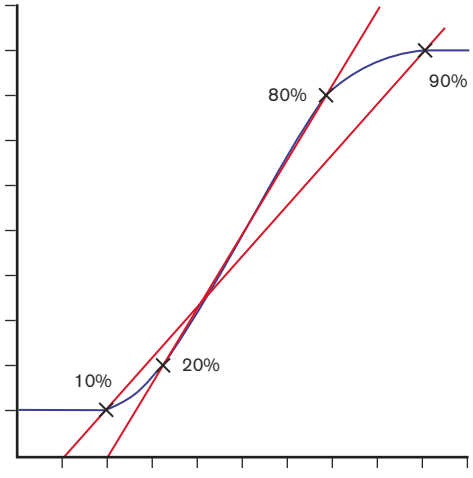

Figure 2 Slew values are more accurate when a trip point lies in the linear region of 20 to 80% of the switching waveform than when it lies in the nonlinear region of 10 to 90%.

thresholds, timing tools calculate the time difference between the driver reaching 50% of its logic-high value and the load reaching 50% of its logic-high value after taking into account slew degradation, which the net causes (**Figure 3**). Similar explanations hold true for falling signals and delays from the input to the output of a cell. Timing tools then calculate slew values from a number of variables outlined in .lib. files. When an interface has different trip points, however, things get a bit more interesting.

Figure 4a depicts a situation in which a driver's delay trip point is 20% and the load-cell trip point is 50%. In such a case, a signal could quickly reach the driver at its delay-trip-point value and arrive slowly at the trip point for the load signal. Hence, the net delay for such an interface can be more than in a situation when the driver is also 50%. Timing tools calculate this extra delay using linear or nonlinear scaling (see **sidebar** "Types of scaling").

Conversely, when a driver's trip point is 50% and its load cell trip point is 20%, the loading signal reaches its delay-trip-point value much sooner than it reaches the trip point for the driver signal (**Figure 4b**). This situation can result in a "negative delay" due to timing tools' linear and nonlinear scaling features. Although you cannot move backward in a time domain, the timing tool must take this delay into account so that the overall path delay from the signal's starting point—in this case, the input pin of the driver cell—to the endpoint—in this case, the output pin of the load cell—is close to the real-world delay, which you can determine using Spice.

Users must also take into account several miscellaneous issues associated with trip points. First, if timing tools encounter negative delays, it is likely that those same negative delays will make their way into the SDF (standard-delay-format) file engineers use for gate-level simulations. Gate-level simulators can't handle negative delays. They either flag an error message or annotate a zero delay for such cases. To work around the problem, designers can write a script to adjust the load- or driver-cell delay in accordance with the calculated negative net delay. **Listing 2**, which is available at www.edn.com/ms4272, contains this script.

Another issue involves calculating the delay between the port and the bidirectional pad pin of I/O cell. Because the net running from the port to the pad pin of the I/O cell is typically outside the chip because the net is a bond wire, a timing tool must still take the delay of the net into account. This approach is complicated, because there is no accurate physical

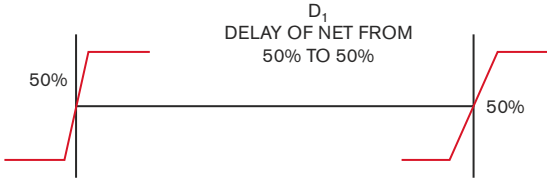

Figure 3 When both the driver and the load have the same delay thresholds and both have equal timing, timing tools calculate the time difference between the drive's reaching 50% of its logic-high value and the load's reaching 50% of its logic-high value.

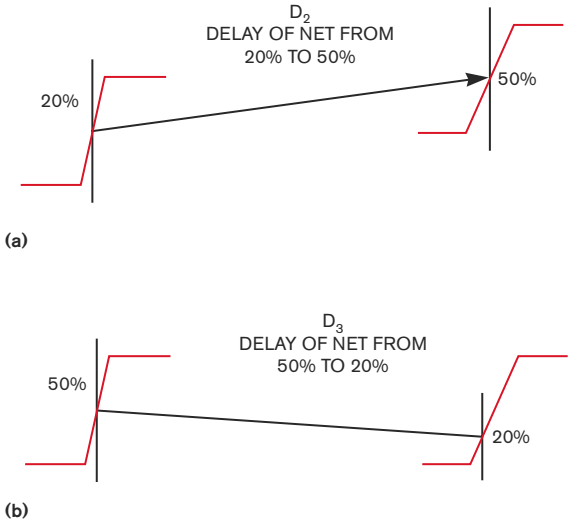

Figure 4 When a driver's delay trip point is 20% and the load-cell trip point is 50%, a signal could quickly reach the driver at its delay-trip-point value and slowly arrive at the trip point for the load signal (a). When a driver's trip point is 50% and its load-cell trip point is 20%, the loading signal more quickly reaches its delay trip-point value than it reaches the trip point for the driver signal (b).

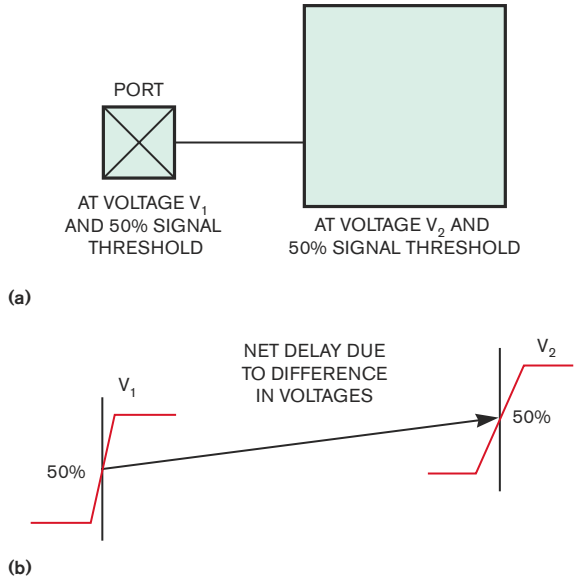

Figure 5 Without a timing model available for the ports, users must manually define a default trip point and voltage level to help the tool calculate the delays.

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information for the net. Without a timing model available for the ports, users must manually define a default trip point and voltage level to help the tool calculate the delays (**Figure 5**). To manually define a default trip point and voltage level, users should first define the operation conditions for ports that are the same as that of I/O cells and then write a script to annotate zero delay for such nets.

It is common to find that libraries are missing trip points. A timing model that does not contain trip-point-threshold or voltage-level values, may have incorrect delays for interfaces to and from them. Because timing tools need at least default values of trip points and voltage levels for analyzing such paths, engineers should consult with their library teams to define the missing trip points.

TIMING-TOOL QUIRKS

A timing tool may fail to perform scaling, resulting in silicon failures because the calculated delays do not match the Spice results. This problem has no easy solution, but it is good practice is to perform Spice analyses for all interfaces that have different trip points. Another method is to use the same trip points for all the modules (hard blocks) in an SOC.

A Spice analysis for multithreshold paths is always a good idea to garner more confidence while cleaning up timing issues. Although thresholds do not exist in the Spice world, the timing models mention them to facilitate the use of timing-analysis tools.

Timing tools typically include a feature that allows users to dump timing paths in the form of a Spice netlist into a Spice tool. To complete this task, users must also provide the Spice tool with a stimulus file containing the input vectors. Spice-simulation tools can read the dumped Spice netlist and the Spice netlists of the standard cells and hard blocks and then source the stimulus file to simulate the critical paths. Engineers need to analyze the generated waveforms to determine whether the path meets timing. One thing to keep in mind while measuring the delay and transition values of such paths in Spice is to use the same trip points that the timing models mention. This approach ensures accuracy.

To properly perform IC-timing analysis, engineers must become familiar with trip points, their nuances, and how timing tools handle them. Failing to properly understand trip points can mean big headaches for a design team and even cause silicon failures. By better studying what they are and how timing tools use them and with a bit of creative script writing, engineers can use trip points to get the most out of their timing methodologies. EDN

TYPES OF SCALING

Most of the industry-standard timing tools use either linear of nonlinear scaling as their modus operandi. In linear scaling, the tool assumes a linear ramp at both thresholds. This method uses the concept of similar triangles to scale the delay from driver to load cell. In nonlinear scaling, tools use current-source models to define the ramps. Calculating the delays requires complex mathematical equations.

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AUTHOR'S BIOGRAPHIES

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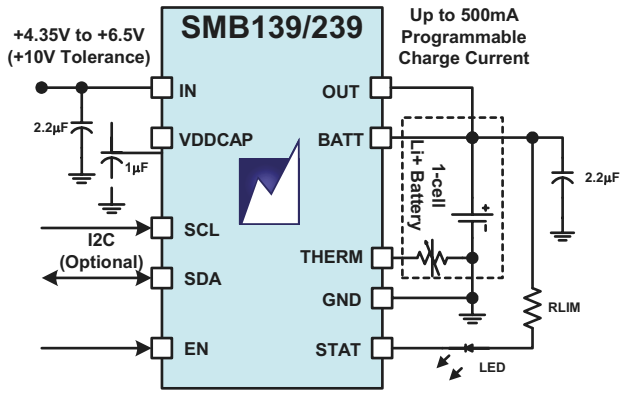

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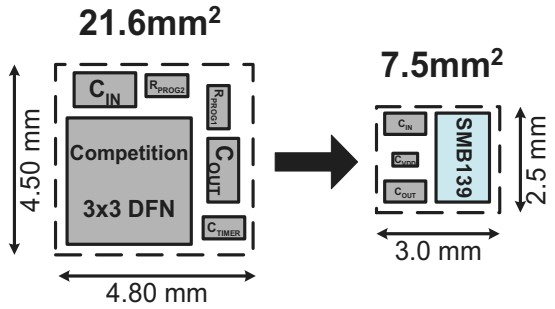

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TurboCharge™ Output	Automatic	Automatic	Software/uC	
CurrentPath™ Control	X			
USB On-The-Go Power	X	X		
Low-Battery Recovery Mode	X			
I2C Interface	X	X	X	X
Programmable Float Voltage	X	X	X	X
Programmable Charge/Term. Current	X	X	X	X
Programmable Input Current Limit	X	X		
Input/Battery OV/UV	X	X	X	X
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Software Watchdog Timer	X	X		
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IC Thermal Protection	X	X	X	X
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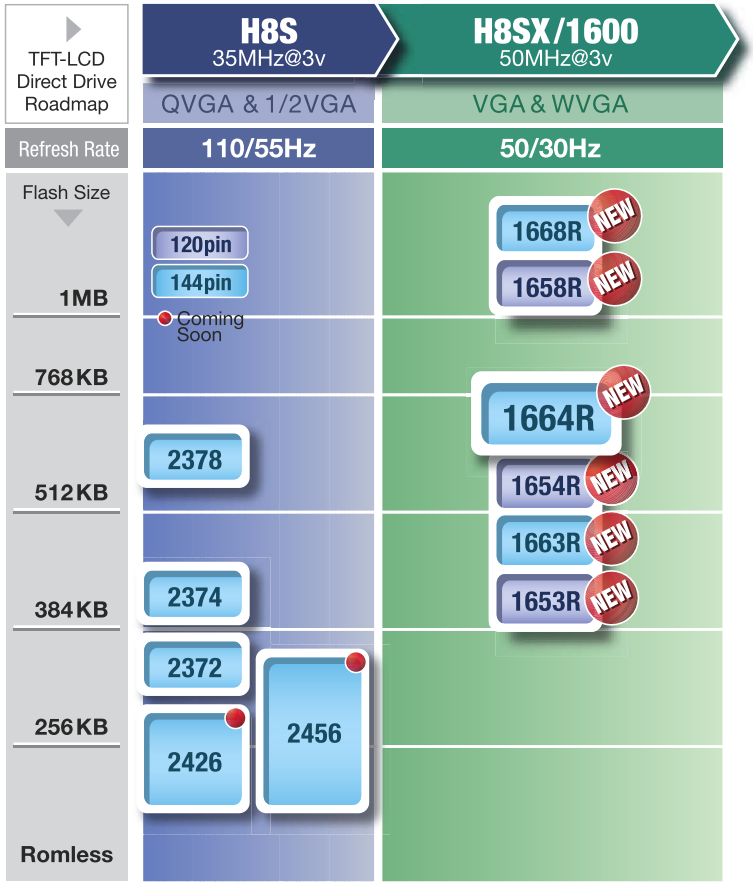

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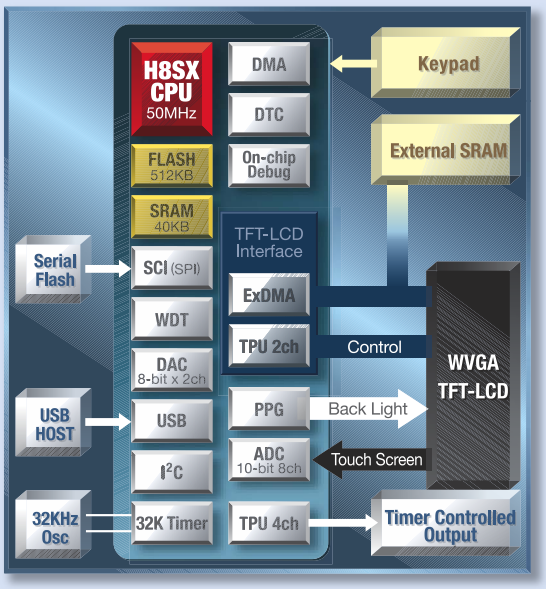

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*Source: Gartner (March 2007) "2006 Worldwide Microcontroller Vendor Revenue" GJ07168

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  - 2800 V/μs slew rate
- Low distortion: –91 dBc @ 10 MHz (G = +1, RL = 1 kΩ)
- Low power: 5 mA per amplifier @ 10 V
- Low noise: 4.4 nV/√Hz
- Wide supply voltage range: 5 V to 10 V
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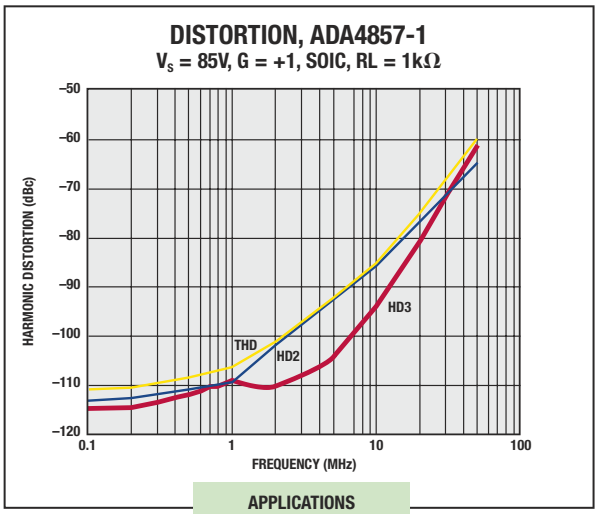

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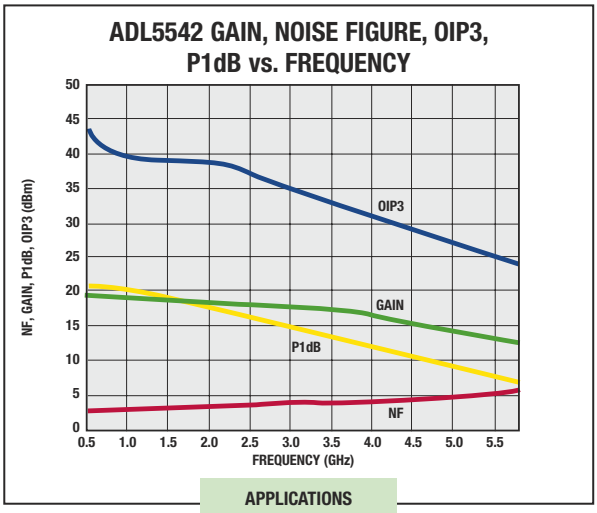

The ADL5541 and ADL5542 are broadband gain blocks ideal for a wide variety of cellular, CATV, medical, and instrumentation equipment. Both devices are 50 Ω internally matched with integrated active bias circuitry, which minimizes the need for external components. The ADL5541 provides 15 dB of gain with an output linearity of 44 dBm at 500 MHz. The pin-compatible ADL5542 provides 20 dB of gain with an output linearity of 46 dBm at 500 MHz.

Compared to other gain blocks currently available, the ADL5541 and ADL5542 offer the highest linearity over frequency, the lowest noise figures, and function across a broader operating frequency range. Both devices are Class 1C (±1 kV) ESD-rated and are available in small footprint LFCSP packages. Fully populated evaluation boards are available from Analog Devices.

APPLICATIONS
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- Satellite equipment
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ADL5542 $1.65

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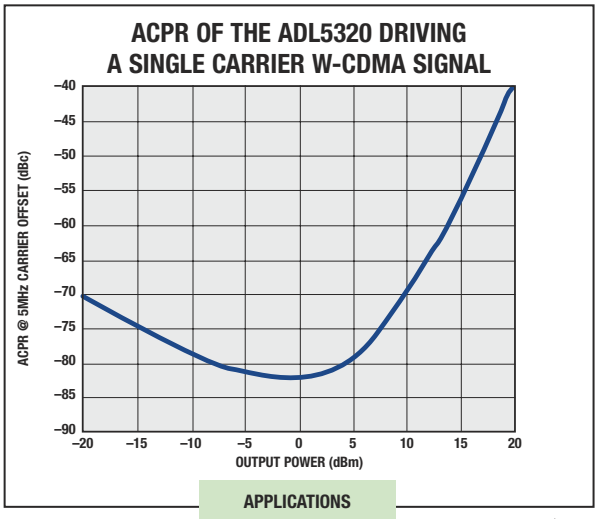
ADL5541	50 to 6000	14.7	39.2 @ 0	16.3	3.8	90	2000	3 mm × 3 mm, 8-lead LFCSP
ADL5542	50 to 6000	18.7	39.0 @ 0	18.0	3.2	93	2000	3 mm × 3 mm, 8-lead LFCSP

RF Drivers Offer Superior Performance While Consuming Less Power

ADI's ADL5320 (400 MHz to 2700 MHz) and ADL5321 (2300 MHz to 4000 MHz) RF driver amplifiers offer very high linearity for a given output power, enabling low distortion and high output drive directly to the power amplifier stages. The ADL5320 provides an output linearity of 42 dBm and a 26 dBm output compression point while consuming just 104 mA of supply current.

The ADL5321 provides an output linearity of 40 dBm and a 25 dBm output compression point while consuming only 84 mA of supply current. Unlike competing devices, Analog Devices' driver amplifiers require minimal external tuning and feature internal active biasing to further minimize the need for external components. Both devices are Class 1C (±4 kV) ESD-rated and are available in a SOT-89 package. Fully populated evaluation boards are available.



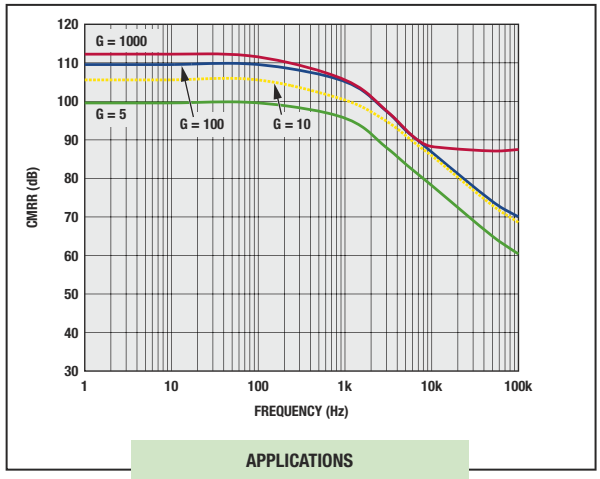
APPLICATIONS
- 3G and 4G wireless
- Broadcast equipment
- Satellite equipment
- Instrumentation

ADL5320 $2.55
ADL5321 $2.55

Part Number	Frequency Range (MHz)	Gain (dB)	OIP3 @ P_{OUT} (dBm)	OP1dB (dBm)	NF (dB)	5 V Current (mA)	Specs @ (MHz)	Package
ADL5320	400 to 2700	13.7	42.0 @ 10	25.6	4.2	104	2140	SOT-89
ADL5321	2300 to 4000	13.8	39.7 @ 10	24.9	4.1	84	2600	SOT-89

Integrated Single-Supply, Rail-to-Rail Instrumentation Amplifier Packs Performance

The AD8223 is a low cost, integrated single-supply instrumentation amplifier (in-amp) that delivers rail-to-rail output swing on a single supply (3 V to 25 V). The device offers superior user flexibility by allowing single-gain set resistor programming. With no external resistor, the AD8223 is configured for G = 5; with an external resistor, the AD8223 can be programmed for gains up to 1000. The AD8223 has a wide input common-mode range and can amplify signals with a common-mode voltage 150 mV below ground. It is available in 8-lead MSOP and SOIC packages with an operating temperature range of –40°C to +85°C.



AD8223 Features

- Gain = 5 to 1000, gain set with 1 resistor
  - 25 nA maximum input bias current
  - 30 nV/√Hz, RTI noise @ 1 kHz
- Power supplies:
  - ±2.5 V to ±12.5 V (dual)
  - 3 V to 25 V (single)
  - 600 μA maximum supply current
- Power consumption: 1.5 mW @ 3 V

APPLICATIONS

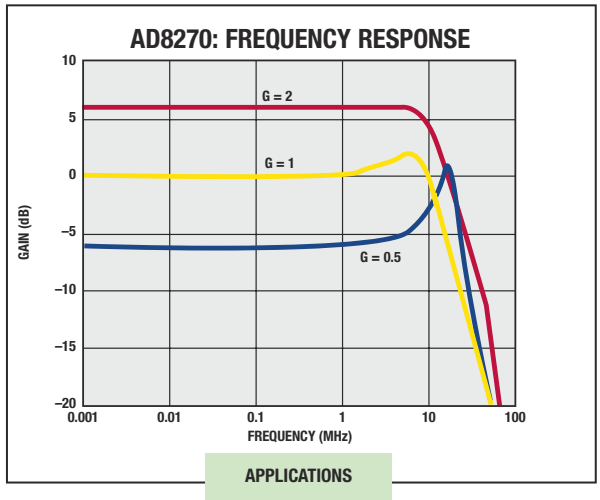
- Battery-powered applications
- Low power medical instrumentation
- Transducer interface
- Thermocoupler amplifiers
- Industrial process controls
- Difference amplifiers

AD8223 $1.15

"In-Amps: How and When to Build Them" at *www.analog.com/onlineseminars/inampbuild*.

Dual Difference Amplifier Offers Higher System Performance and Channel Density at an Attractive Price

The AD8270 is a dual-channel, pin-programmable difference amplifier with internal gain setting resistors that offer unmatched dc precision with ac bandwidth specifications. The device combines 10 MHz of bandwidth and a 30 V/μs slew rate, making it ideally suited for advanced applications such as high speed industrial control measurement and multichannel systems where high bandwidth and SNR are required. With no external components, the AD8270 can be configured as a high performance difference amplifier (G = 0.5, 1, or 2), inverting amplifier (G = 0.5, 1, or 2), or noninverting amplifier (G = 1.5, 2, or 3). It is offered in a 4 mm × 4 mm, 16-lead LFCSP, supporting double the channel density at a lower cost per channel vs. competitive solutions with no compromise in performance. A standard pinout 14-lead SOIC (G = 0.5 or 2) version of this device, the AD8273, is also available.



Both the AD8270 and AD8273 operate on single and dual supplies and only require 2.5 mA maximum supply current per amplifier. Each device is fully ROHS compliant and is specified over the industrial temperature range of –40°C to +85°C. The AD8270's dc accuracy, when combined with a high slew rate, makes it an optimal ADC driver for ADI's broad portfolio of PulSAR® ADCs that includes the AD7980 and AD7688. The ADR43x and ADR36x low noise voltage references, with sync and source capabilities, are recommended compatible products for the AD8270 and AD8273 difference amplifiers.

AD8270 and AD8273 Features

- Bandwidth: >10 MHz
- Slew rate:
  - 30 V/μs (AD8270)
  - 20 V/μs (AD8273)
- Gain accuracy: 0.05%
- Gain drift: 10 ppm/°C
- Offset voltage: 700 μV
- CMRR: 86 dB

APPLICATIONS

- High performance audio
- Instrumentation amplifier building block
- Level translator
- Automatic test equipment
- Sine/cosine encoders

AD8270 (16-lead LFCSP) $1.89
AD8273 (14-lead SOIC) $1.65

For samples and data sheets, visit www.analog.com/V8Amplifiers

Low Noise Amplifiers

Part Number	V_{SY} (V)	V_{OS} Max (µV)	BW (MHz)	Slew Rate (V/µs)	I_{SY}/ Amp Max (mA)	e_N @ 1 kHz (nV/√Hz)	I_B Max (nA)	CMRR Min (dB)	PSRR Min (dB)	Number of Amps	Package	Price ($U.S.)
Precision Operational Amplifiers												
AD797	10 to 36	40	8	20	10.5	0.9	900	120	120	1	PDIP, SOIC	4.74
AD8599	9 to 36	120	10	15	5.7	1.07	180	120	120	2	SOIC	3.20
ADA4004-4	10 to 36	140	12	2.7	1.8	1.8	85	105	110	4	SOIC, LFCSP	3.06
AD8676	10 to 36	50	10	2.5	2.7	2.8	2	105	106	2	SOIC, MSOP	1.64
AD8675	10 to 36	75	10	2.5	2.7	2.8	2	105	120	1	SOIC, MSOP	1.17
OP27	8 to 44	25	8	2.8	5.7	3	40	114	100	1	TO-99, CerDIP, PDIP, SOIC	1.18
OP37	8 to 44	25	12	17	5.7	3	40	114	100	1	CerDIP, PDIP, SOIC	1.13
OP270	9 to 36	75	5	2.4	3.25	3.2	20	106	110	2	CerDIP, PDIP, SOICW	2.77
OP470	9 to 36	400	6	2	2.75	3.2	25	100	105	4	CerDIP, PDIP, SOICW	4.38
AD743	9.6 to 36	1000	4.5	2.8	10	3.2	400	80	90	1	SOIC, PDIP	5.26
AD745	9.6 to 36	500	20	12.5	10	3.2	250	90	100	1	SOIC	5.01
AD8671	10 to 36	75	10	4	3.5	2.8	12	100	110	1	SOIC, MSOP	1.05
AD8672	10 to 36	75	10	4	3.5	2.8	12	100	110	2	SOIC, MSOP	1.70
AD8674	10 to 36	75	10	4	3.5	2.8	12	100	110	4	SOIC, TSSOP	3.20
OP184	3 to 36	65	3.25	2.4	1.45	3.9	450	86	76	1	SOIC	1.64
OP284	3 to 36	65	3.25	2.4	1.45	3.9	450	86	76	2	PDIP, SOIC	2.97
OP484	3 to 36	75	3.25	2.4	1.45	3.9	450	86	76	4	PDIP, SOIC	4.95
AD8655	2.7 to 6	250	28	11	4.5	4	0.01	85	88	1	SOIC, MSOP	0.70
AD8656	2.7 to 6	250	28	11	4.5	4	0.01	85	88	2	SOIC, MSOP	1.10

Noise Optimization in Sensor Signal Conditioning Circuits

Part I of this online seminar covers the types, sources, characteristics, and analysis techniques of noise; and introduces a low noise design process—available at *www.analog.com/onlineseminars/noise1*.

Part II will walk you through the entire low noise design process and show how to manage noise to meet required signal chain performance objectives. Design dos and don'ts, as well as a number of circuit optimization techniques, will be presented—available at *www.analog.com/onlineseminars/noise2*.

Low Noise Amplifiers (Continued)

Part Number	V_{SY} (V)	V_{OS} Max (μV)	BW (MHz)	Slew Rate (V/μs)	I_{SY}/ Amp Max (mA)	e_N @ 1 kHz (nV/√Hz)	I_B Max (nA)	CMRR Min (dB)	PSRR Min (dB)	Number of Amps	Package	Price ($U.S.)
Precision Operational Amplifiers (Continued)												
OP113	4 to 36	75	3.4	1.2	3	4.7	600	96	100	1	SOIC	1.74
OP213	4 to 36	100	3.4	1.2	3	4.7	600	96	100	2	PDIP, SOIC	2.08
OP413	4 to 36	125	3.4	1.2	3	4.7	600	96	100	4	SOIC	4.47
SSM2135	4 to 36	2000	3.5	0.9	3	5.2	750	87	90	2	SOIC	2.57
OP285	9 to 44	250	9	22	2.5	6	350	80	85	2	SOIC	2.37
AD8610	10 to 27	100	25	50	3	6	0.01	90	100	1	SOIC, MSOP	3.71
AD8620	10 to 27	150	25	50	3	6	0.01	90	100	2	SOIC	7.41
OP275	9 to 44	1000	9	22	2.5	6	350	80	85	2	SOIC, PDIP	0.99
OP467	9 to 36	500	28	170	2.5	6	600	80	96	4	CerDIP, PDIP, SOIC, LCC	7.39
OP471	9 to 36	2500	6.5	8	2.75	6.5	60	95	95	4	SOIC	4.87
OP1177	5 to 36	60	1.3	0.7	0.5	7.9	2	120	120	1	SOIC, MSOP	0.80
OP2177	5 to 36	75	1.3	0.7	0.5	7.9	2	120	120	2	SOIC, MSOP	1.51
OP4177	5 to 36	75	1.3	0.7	0.5	7.9	2	120	120	4	SOIC, TSSOP	3.56

Part Number	V_{SY} (V)	BW (MHz)	Slew Rate (V/μs)	Noise (nV/√Hz)	Distortion SFDR @ BW		V_{OS} Max (mV)	I_B Max (μA)	I_{SY}/Amp Typ (mA)	Package	Price ($U.S.)
					dBc	MHz					
High Speed Operational Amplifiers											
ADA4841-1, ADA4841-2	2.7 to 12	80	12	2.1	–105	0.1	0.3	5.3	1.1	SOT-23, MSOP, SOIC	1.59, 2.29
ADA4899-1	4.5 to 12	600	310	1	–80	10	0.23	1	14.7	LFCSP, SOIC	1.89
AD8021	4.5 to 24	205	150	2.1	–93	1	1	10.5	7	SOIC, MSOP	1.29
AD8022	4.5 to 26	130	50	2.5	–95	1	6	5	4	SOIC, MSOP	2.35
AD8045	3.3 to 12	1000	1350	3	–90	20	1	6.3	16	LFCSP, SOIC	1.39
AD8099	4.5 to 12	700	1350	0.95	–84	10	0.5	2	15	LFCSP, SOIC	1.98
Differential Amplifiers											
ADA4937-1, ADA4937-2	3 to 5.25	1900	6000	2.2	–84	70	2.5	30	39.5	LFCSP	3.79, 5.69
ADA4938-1, ADA4938-2	4.5 to 11	1000	4700	2.6	–82	50	4	18	37	LFCSP	3.79, 5.69
ADA4922-1	5 to 26	38	260	12[1]	–99	0.1	1.1	3.5	9.4	LFCSP, SOIC	3.59
ADA4941-1	2.7 to 12	32	26	10.2[1]	–109	0.1	0.8	4.5	2.5	LFCSP, SOIC	2.39
AD8139	4.5 to 12	410	800	2.25	–98	1	0.5	8	24.5	LFCSP, SOIC	3.59

[1]RTO

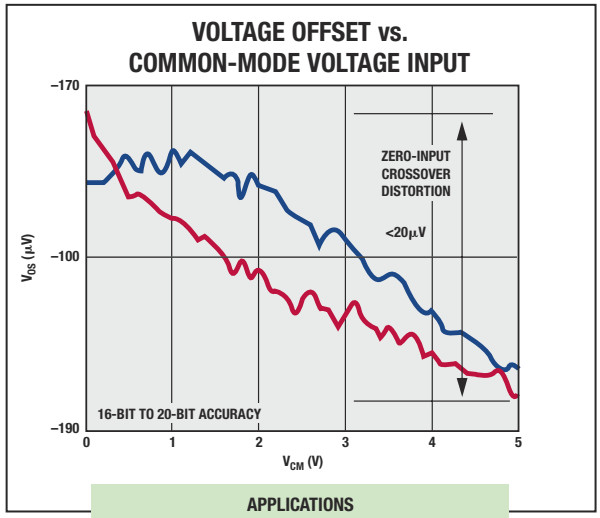
Low Noise Amplifiers (Continued)

Part Number	V_{SY} (V)	Gain Setting Method	BW kHz (G = 10)	Gain Min (dB)	Gain Max (dB)	Min CMRR 60 Hz Min Gain (dB)	Min CMRR 60 Hz Max Gain (dB)	V_{NOISE} RTI 1 Hz to 10 Hz (μV p-p)	Package	Price ($U.S.)
Instrumentation Amplifiers										
AD8220	4.6 to 36	Resistor	800	1	1000	78	94	0.8	MSOP	2.29
AD8221	4.6 to 36	Resistor	562	1	1000	80	130	0.25	MSOP, SOIC	1.99
AD8222	4.6 to 36	Resistor	750	1	10000	80	130	0.25	LFCSP	3.59
AD8224	4.6 to 36	Resistor	800	1	1000	78	94	0.8	LFCSP	4.12
AD8250	10 to 34	Pin, software	3000	1	10	80	98	1	MSOP	4.95
AD8251	10 to 34	Pin, software	2500	1	8	80	98	1.2	MSOP	4.95

Part Number	V_{SY} (V)	Gain Control	–3 dB BW MHz (G = 10)	Gain Min (dB)	Gain Max (dB)	Number of Amps	Spectral Noise (nV/√Hz)	Supply Current Max (mA)	Gain Accuracy	OP1dB (dBm)	Package	Price ($U.S.)
Variable Gain Amplifiers												
AD8331	4.5 to 5.5	Analog	120	–4.5	43	1	0.74	25	0.5	7	QSOP	5.39
AD8332	4.5 to 5.5	Analog	120	–4.5	43.5	2	0.74	58	0.5	7	TSSOP, CSP	10.44
AD8334	4.5 to 5.5	Analog	100	–4.5	43.5	4	0.74	116	0.5	7	LFCSP	14.49
AD8335	4.5 to 5.5	Analog	70	–10	38	4	1.3	76	±0.2	7	LFCSP	12.00
AD8336	±3 to ±12	Analog	115	–14	46	1	3	25	±0.5	11	LFCSP	4.59
AD8337	4.5 to 10	Analog	280	0	24	1	2.2	15	±0.25	14.5	LFCSP	2.49

20 μA Max, R-R I/O, Zero-Input Crossover Distortion Amplifier

The AD8506 is a high performance, dual CMOS amplifier that boasts 105 dB CMRR. The device offers zero crossover distortion for 16-bit accuracy and very low input bias current while operating with a supply current of less than 20 μA per amplifier. The AD8506 offers the lowest noise in its power class. It is specified for both the industrial temperature range of –40°C to +85°C and the extended industrial temperature range of –40°C to +125°C. It will be available in an 8-lead WLCSP in mid 2008.



AD8506 Features

- I_{SY}: 20 μA max
- CMRR: 105 dB typ
- PSRR: 100 dB min
- Offset voltage: 2.5 mV max
- Offset drift: <2 μV/°C

APPLICATIONS

- Pressure and position sensors
- Remote security
- Biosensors
- IR thermometers
- Battery-powered consumer equipment
- Hazard detectors

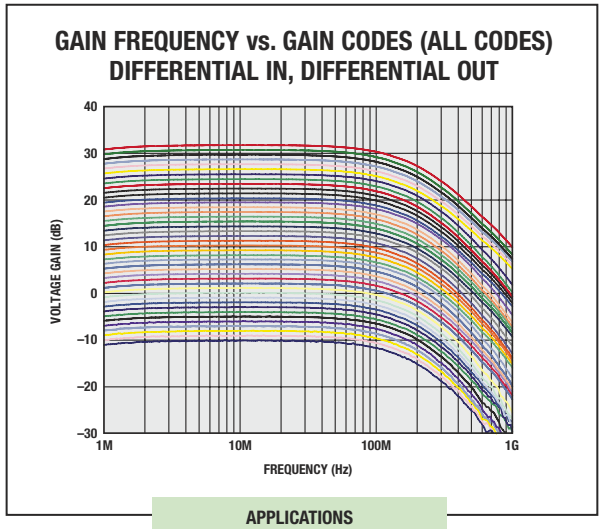
AD8506 $0.70

Dual, Digitally Controlled Variable Gain Amplifier (VGA) for CMTS Upstream Receivers

The AD8372 is a dual-channel, digitally controlled variable gain amplifier (VGA) developed specifically for CMTS upstream receiver applications. It is flexible and easy to use while offering accuracy, gain control, linearity, and low noise. Each channel is independently controlled by serial 8-bit SPI interfaces providing a readback function for verification of the target gain setting. Serial control reduces the pin count and allows the AD8372 to be packaged in a 5 mm × 5 mm, 32-lead LFCSP.

AD8372 Features

- Differential input: 150 Ω; open-collector differential output
- 7.8 dB noise figure to 100 MHz @ maximum gain
- –3 dB bandwidth of 130 MHz
- Gain range: 41 dB; 1 dB step size (±0.2 dB)
- HD2/HD3 better than 77 dBc for 1 V p-p differential output
- SFDR: >70 dB
- Output IP3 of 35 dBm



APPLICATIONS

- Differential ADC drivers
- CMTS upstream direct sampling receivers
- CATV modem signal scaling
- Generic RF/IF gain stages

AD8372 $6.50

Auto-Zero Amplifiers for Thermopile Sensors in Smart Appliances

The trend toward smarter applications demands less expensive electronic components and sensors. These sensors and analog front ends are used in a variety of appliance applications from detecting temperature distribution in microwave ovens to sensing the dampness of clothes in dryers.

Thermopile sensors incorporate a series of thermoelements that form a sensitive region to produce output voltages in the range of 100 μV to 900 μV. The output signal vs. frequency is fairly constant and is directly proportional to incident radiation. Because measuring these low level thermopile signals imposes great challenges on signal conditioning circuits, a very high precision amplifier, such as an auto-zero amplifier, is recommended. ADI's portfolio of leading auto-zero amplifiers features extremely low offset voltages in the range of tens of microvolts over temperature, as well as very high common-mode rejection to minimize signal distortions.

Part Number	V_{SY} (V)	V_{OS} Max (μV)	TCV_{OS} Max (μV/°C)	GBP (MHz)	I_{SY} Max	e_N @ 1 kHz (nV/√Hz)	CMRR Min (dB)	PSRR Min (dB)	R-R In	R-R Out	Number of Amps	Price ($U.S.)
AD8571, AD8572, AD8574	2.7 to 6	5	0.04	1.5	975 μA	51	120	120	Yes	Yes	1, 2, 4	1.10, 1.76, 3.36
AD8628, AD8629, AD8630	2.7 to 6	5	0.02	2.5	1.1 mA	22	120	115	Yes	Yes	1, 2, 4	0.95, 1.45, 2.70
AD8551, AD8552, AD8554	2.7 to 6	5	0.04	1.5	975 μA	42	120	120	Yes	Yes	1, 2, 4	1.19, 1.88, 3.32
AD8638, AD8639	5	9	0.04	1.35	1.3 mA	60	118	127	No	Yes	1, 2	1.25, 2.19
AD8538, AD8539	2.7 to 6	13	0.1	0.43	180 μA	50	115	105	Yes	Yes	1, 2	0.89, 1.29

ADI Web Design Tools for Amplifier Selection, Evaluation, and Circuit Building

Analog Devices now provides several custom design selection and simulation tools that, when used together, offer even novice designers powerful resources to pinpoint the best design options for their projects.

ADIsimOpAmp™ Evaluation Tool

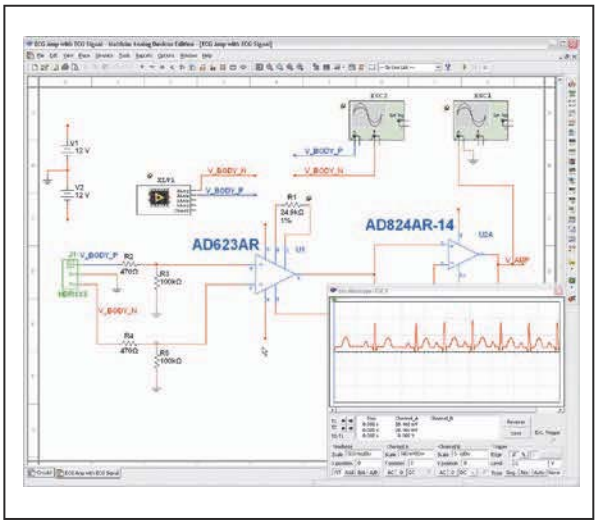
This tool will help with the selection, evaluation, and troubleshooting of voltage feedback op amps. It uses typical data to model the behavior of a selected amplifier. It allows a user to select an amplifier, configure a circuit, apply a signal, and evaluate the performance. It is useful for checking an amplifier's specifications including bandwidth, slew rate, I/O range, gain error, load current, stability issues, and dc errors in a given circuit The tool also employs an embedded version of NI Multisim™ SPICE to provide more detailed response characteristics of a given op amp, such as square wave settling response and capacitive loading analysis. No registration is necessary to check out this tool!

Visit *www.analog.com/ADIsimOpAmp*.

NI Multisim Analog Devices Edition

This free software download is ideal for the next stage as it enables users to simulate their own circuit design. Powered by industry-standard SPICE technology, NI Multisim Analog Devices Edition, codeveloped by National Instruments and Analog Devices, provides an intuitive environment for capturing and simulating analog circuits. It includes over 400 ADI amplifier product models from which to choose and evaluate, as well as dozens of prebuilt circuits demonstrating common building blocks.

Visit *www.analog.com/multisim*.



Screen capture showing NI Multisim Analog Devices Edition in action.

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Printed in the U.S.A. SB07385-90-2/08

BY BRIAN D MATHEWS • XCEIVE CORP

Digital TV for the future: hybrid analog/digital-TV-receiver design

ANALOG TV HASN'T DISAPPEARED YET, SO YOU STILL NEED TO UNDERSTAND IT WHEN DESIGNING HYBRID ANALOG/DIGITAL SYSTEMS.

Analog is rapidly disappearing, but you still need to worry about developing analog-TV receivers because, in most parts of the world, it will be some time before manufacturers eliminate analog TVs. Even then, they may continue to have cable systems that carry analog-TV signals. Smart TV, set-top-box, and PVR/DVR (personal-video-recorder/digital-video-recorder) product developers will plan to include analog in their digital TVs for a long time. To understand hybrid analog/digital-TV-receiver options, you must take a brief look back at the evolution of TV-front-end architectures.

ANALOG-TV ARCHITECTURE

Basic analog TVs receive terrestrial analog-RF (radio-frequency) signals and produce a good picture—not challenging tasks because AM (amplitude-modulation) analog-RF-TV signals require only a moderate-performance noise figure, linearity, phase noise, gain, AGC (automatic-gain-control) response, and frequency stability. Analog-TV-receiver architectures follow a classic heterodyne approach that filters and amplifies the incoming signal and applies it to a mixer (**Figure 1**). The mixer translates the RF signal into an IF (intermediate-frequency) signal, further filters and amplifies it, and presents it to the analog-demodulator blocks.

Making analog-TV products "cable ready" required some changes from these basic performance requirements. Terrestrial-broadcast-TV signals differ greatly from cable signals. The FCC (Federal Communications Commission) allocates a transmitter-frequency band to each TV broadcaster. It bases this allocation on a regional frequency plan that aims to eliminate the presence of strong signals on adjacent channels. This system enables TV receivers to detect the channels of most interest to them—those nearest to the user's home.

The FCC assigns channels to broadcast transmitters in a way that separates the frequency of strong signals, because receivers cannot easily reject interference in close frequency to the desired signal. Otherwise, a high-power signal could reside in the channel adjacent to a desired weak signal and make reception of the weak signal impossible for any practical receiver implementation.

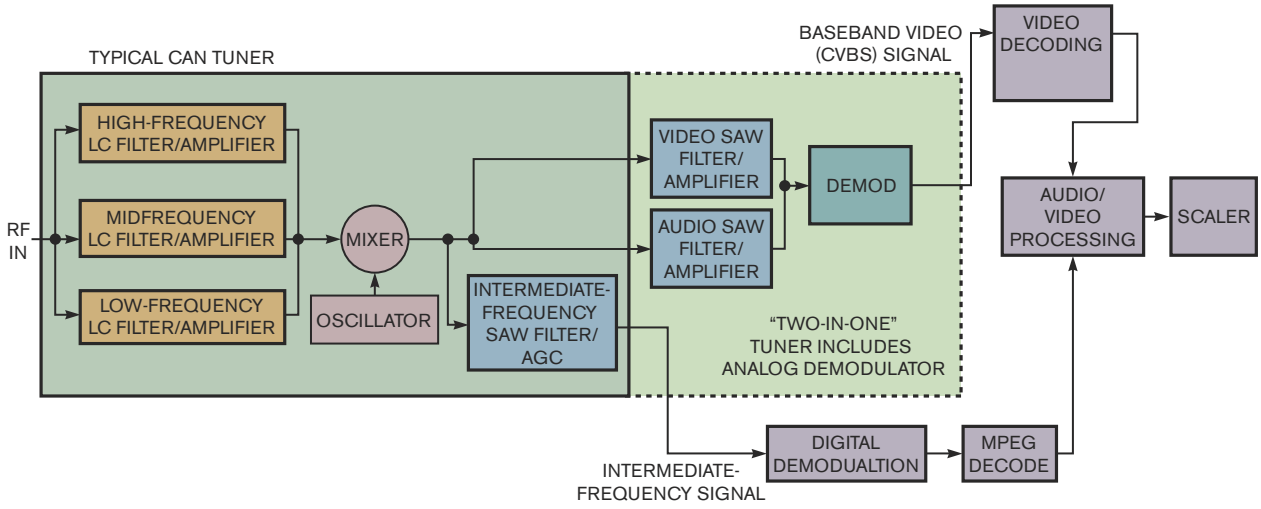

Figure 1 Analog-TV-receiver architectures follow a classic heterodyne approach that filters and amplifies the incoming signal and applies it to a mixer.

In addition to being sparsely spaced in frequency—like a comb with many missing teeth—terrestrial signals that the TV receives have vastly differing power levels because of the varying power levels of transmitters and their proximity to the receiving set. A receiver might be near one transmitter, but it needs to also receive signals from a distant transmitter. TV receivers perform well with off-air signals, which can vary in signal power by nearly three orders of magnitude from milliwatts to microwatts—like a gap-toothed comb with teeth of various lengths.

Conversely, TV signals in a cable system are closely spaced and of relatively equal power—like a new comb—because cable operators must use all of the available spectra to offer as many channel options as possible and the cable medium shields the signals from outside interference. And, because one transmitter generates the signals, cable systems can control the signal levels. Thus, a signal on an adjacent channel cannot be much stronger than a signal on the other channel.

To make an analog TV cable ready simply means that it must deal with closely spaced, equal-level signals and must use all the channels. An RF receiver handling this type of signal must have better linearity than a receiver for terrestrial analog receivers. RF linearity generally has 1-dB compression and third-order intercept, but, because of the many channels in cable systems, the TV industry has developed TV-specific parameters: CSO (composite-second-order) and CTB (composite-triple-beat) parameters for specifying a receiver's resistance to intermodulation effects. Tuner products for use in cable-ready TVs will include these specifications.

THE RISE OF DIGITAL TV

A simple digital-TV architecture would include a receiver section for digital-terrestrial signals. Digital-TV standards bodies have developed specifications, such as the ATSC (Advanced Television Systems Committee) A/74, that receivers must meet to provide good reception of the new digital-TV signals. Generally, the digital-terrestrial-TV receivers have a better noise figure, overall gain, selectivity, linearity, and AGC range and response than their analog counterparts. Digital-tuner modules offer these specifications. However, most early hybrid analog/digital-TV designs used two tuner modules—one for receiving analog signals and the other for receiving digital signals. This approach increased the cost, size, and power consumption of the designs. On the other hand, it also allowed designers to include additional filtering, amplification, or both to either the digital or the analog tuner to further increase performance. Most digital TVs also included two threaded, F-type RF connectors with "analog," "digital," "air," and "cable" labels.

To keep up with flat-panel TV screens, TV developers must work with constantly shrinking PCBs (printed-circuit boards). A hybrid tuner and RF switch provide dual inputs with a single tuner module. More recently, designers have developed hybrid analog/digital-capable tuner modules. These new designs provide the performance for DTV and meet the demanding requirements of TV manufacturers for analog-terrestrial and cable reception. New TV designs employ these modules, sometimes with an RF switch so that dual input connectors could still be available at the back of the TV. In some cases, the TV manufacturer adds application-specific gain or filtering between the tuner module and the connector to enhance the receiver performance. These types of designs frequently include low-noise amplifiers that provide additional gain to achieve better sensitivity when the system is operating in digital mode.

Digital-cable systems generally employ set-top boxes from

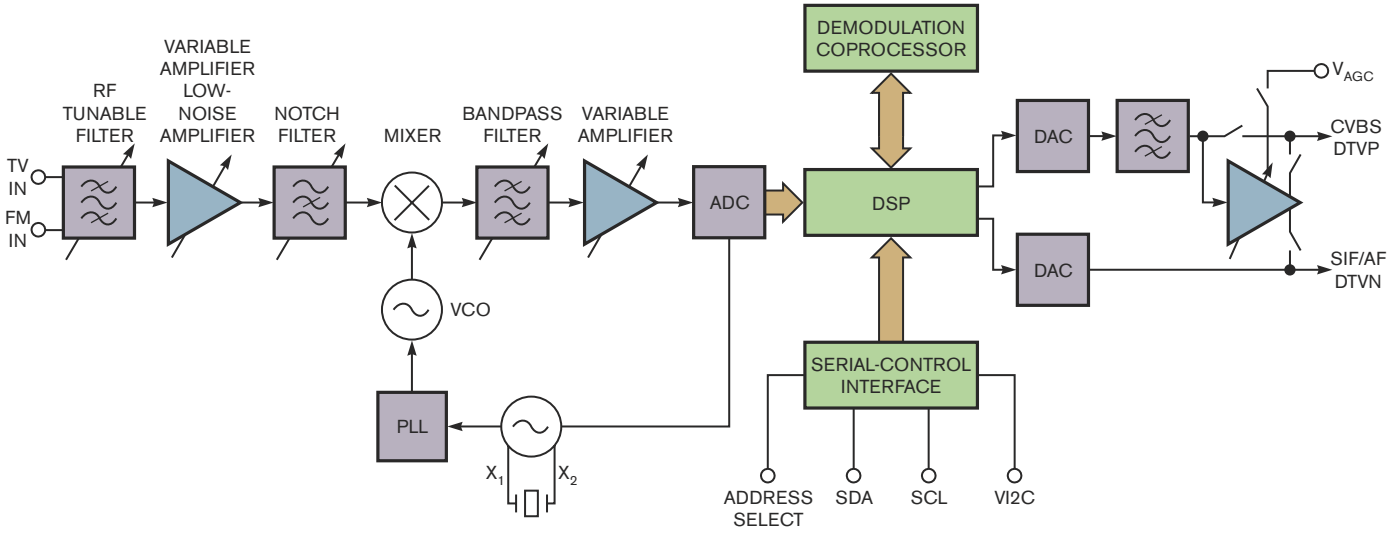

Figure 2 Monolithic silicon tuners offer performance meeting the rigorous requirements of leading TV manufacturers and also integrate all the hybrid-TV-receiver functions, including the analog demodulation, in a 7×7-mm surface-mount package with substantially lower power consumption than currently available CAN modules.

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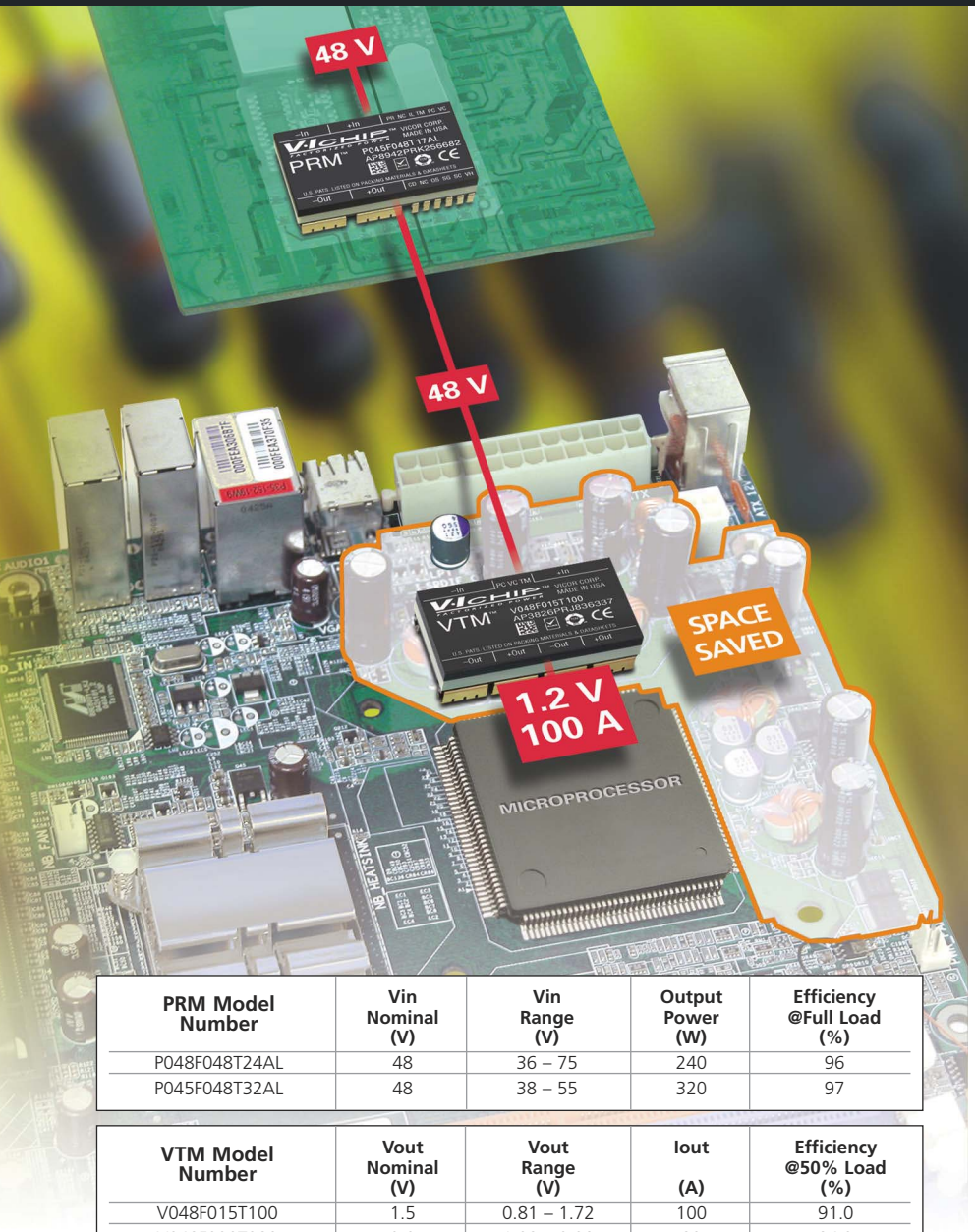

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P045F048T32AL	48	38 – 55	320	97

VTM Model Number	Vout Nominal (V)	Vout Range (V)	Iout (A)	Efficiency @50% Load (%)
V048F015T100	1.5	0.81 – 1.72	100	91.0
V048F020T080	2.0	1.08 – 2.29	80	94.2
V048F040T050	4.0	2.17 – 4.58	50	94.8
V048F120T025	12.0	6.50 – 13.75	25	95.1

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the cable company. However, TV manufacturers have developed "digital-cable-ready" and "clear-QAM" (quadrature-amplitude-modulation)-capable TVs that allow users to directly connect TVs to digital-cable systems without a set-top box. This feature requires the use of RF-receiver electronics to add reception of complex high-order QAM signals. Other requirements include the need to meet analog-off-air, analog-cable, and digital-off-air specifications. Digital-cable signals are the most complex signals to receive. Thus, designers must address new, critical specifications, such as digital sensitivity, adjacent-channel rejection, and phase noise, to meet digital-cable requirements. The newest tuner-module products in the latest DTV designs meet all of these requirements.

Analog-TV designers usually include the demodulator as part of the tuner module. Many tuner-module products are available that provide analog demodulation, although TV manufacturers sometimes select RF-only tuners and implement the analog-demodulation function with discrete components that they mount on the TV's main board between the tuner and the video/audio-processing blocks. Hybrid-tuner modules also include the analog-demodulation function. In analog mode, the outputs are CVBS (composite-vertical-blanking-signal) baseband video and SIF (sound intermediate frequency). Digital mode uses different filter- and AGC-amplifier sections, and a narrowband digital-mode IF acts as the output to a digital demodulator. Some people refer to this type of hybrid-tuner module as a two-in-one tuner, indicating that it includes both a tuner and an analog demodulator.

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The ideal approach, however, would be a single block that would perform well in both analog/digital and terrestrial/cable modes. Manufacturers have long offered bulky tuner CAN (controller-area-network) modules that address this goal. These modules, which find use in many current TV designs, comprise many discrete parts, including multiple ICs, small surface-mount passives, variable capacitors, and multiple air-coil inductors. Due to the size, power consumption, and complexity of these modules, designers are seeking out alternatives.

ENTER SILICON-TUNER ICs

One approach is to place RF-only tuner modules and select discrete SAW (surface-acoustic-wave) filters and analog-demodulator ICs next to the tuner module on a TV's main board. This approach allows the designer to select the best components but also increases the main board's chip count and could require fine-tuning and board redesigns. The ideal approach would employ one chip that offers all the performance and integration of the hybrid two-in-one tuner modules. Although monolithic silicon-tuner ICs have for several years been available, they have only recently been able to match the performance and integration of modules. Monolithic silicon tuners have not found wide use in TV applications due to the difficulties in simultaneously meeting all the demands of analog and digital, terrestrial and cable, and tuning and demodulation at the levels that TV manufacturers require.

However, new silicon-tuner ICs from TV-tuner manufacturers are meeting both the integration and the performance levels of CAN-tuner modules. New models appearing on the market in the coming months will demonstrate that monolithic silicon-tuner ICs can meet the rigorous requirements for new hybrid analog/digital-TV designs. These new monolithic silicon tuners offer performance meeting the rigorous requirements of leading TV manufacturers and also integrate all the hybrid-TV-receiver functions, including the analog demodulation, in a 7×7-mm surface-mount package with substantially lower power consumption than currently available CAN modules (**Figure 2**). EDN

AUTHOR'S BIOGRAPHY

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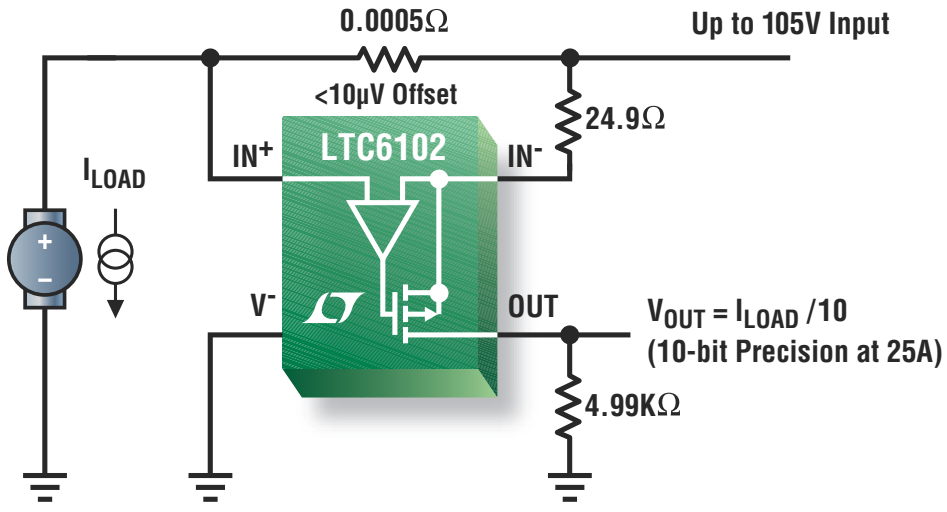
Zero-Drift I_{SENSE}



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Current Sense Amplifiers

	NEW	NEW	NEW	NEW	NEW			
Part	**LT®6106**	**LT6105**	**LTC6104**	**LTC6103 Dual**	**LTC6102 LTC6102HV**	**LTC6101 LTC6101HV**	**LT6100**	**LT1787 LT1787HV**
Current Direction	→	→	↔	→	→	→	→	↔
Common Mode Voltage	2.7V to 44V	-0.3V to 44V	4V to 70V	4V to 70V	4V to 70V 5V to 105V	4V to 70V 5V to 105V	4.1V to 48V	2.5V to 40V 2.5V to 65V
Response Time	3.5µsec	3.5µsec	1µsec	1µsec	1µsec	1µsec	40µsec	10µsec
V_{OS} Max.	250µV	300µV	450µV	450µV	10µV	300µV	300µV	100µV
V_{OS} Drift	1µV/°C	1µV/°C	1.5µV/°C	1.5µV/°C	50nV/°C	1µV/°C	0.5V/°C	0.5V/°C
I_{BIAS} Max.	40nA	25µA	170nA	170nA	3nA	170nA	10µA	20µA
Gain	R-SET	R-SET	R-SET	R-SET	R-SET	R-SET	PIN-SET	8V/V
PSRR Min.	106dB	100dB	110dB	110dB	120dB	118dB	105dB	120dB

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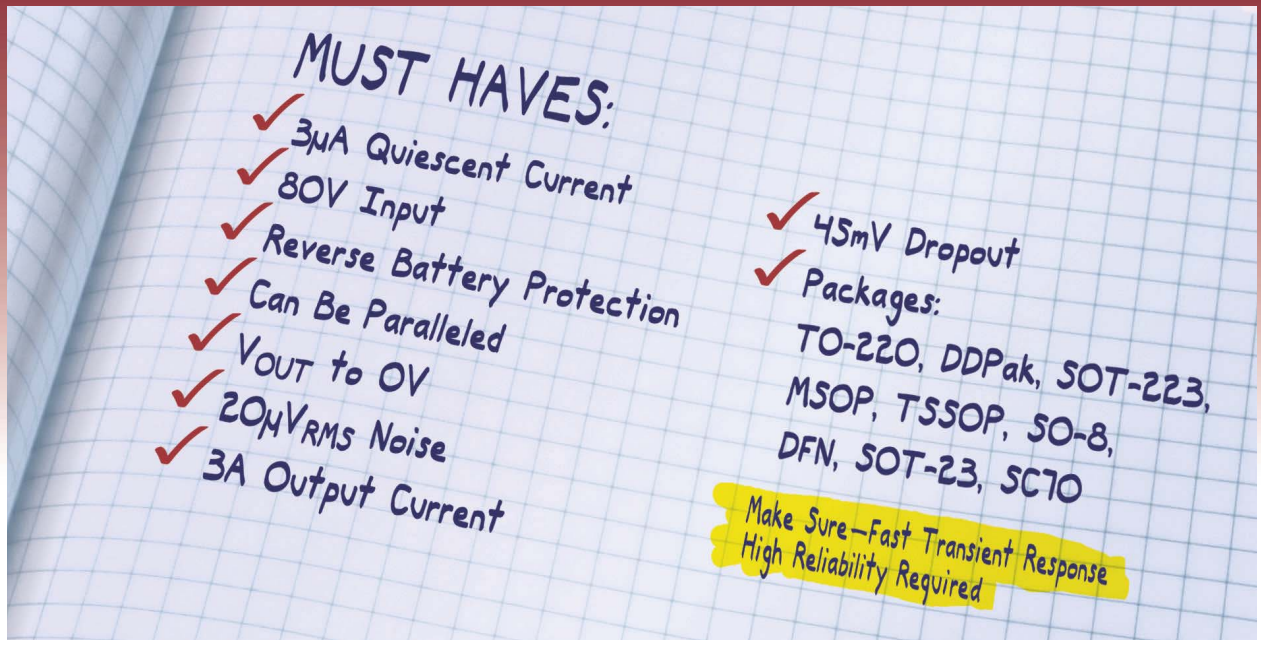

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Part No.	I_{OUT}	Max. V_{IN} (V)	Dropout Voltage (V)	Noise (μV_{RMS})	I_Q	Output Voltage (V)	Package (mm)
LT®3009	20mA	20	0.28	150	3µA	Adj. (0.6 to 19.5)	2 x 2 DFN-6, SC70-8
LT3010/H*	50mA/50mA	80	0.30	100	30µA	Adj. (1.275 to 60), 5	ThinSOT™
LT1761	100mA	20	0.30	20	20µA	Adj. (1.22 to 20), Fixed	ThinSOT
LT1762	150mA	6.5	0.30	20	25µA	Adj. (1.22 to 20), Fixed	MSOP-8
LT3012/H*	250mA/200mA	80	0.40	100	40µA	Adj. (1.24 to 60)	3 x 4 DFN-12, TSSOP-16E
LT3013/H*	250mA/200mA	80	0.40	100	65µA	Adj. (1.24 to 60)	3 x 4 DFN-12, TSSOP-16E
LT1962	300mA	20	0.27	20	30µA	Adj. (1.22 to 20), Fixed	MSOP-8
LTC®3025	300mA	5.5	0.05	80	54µA	Adj. (0.4 to 3.6)	2 x 2 DFN-6
LTC3035	300mA	5.5	0.045	150	100µA	Adj. (0.4 to 3.6), Fixed	2 x 2 DFN-6
LT1763	500mA	20	0.30	20	30µA	Adj. (1.22 to 20), Fixed	SOIC-8
LTC3025-1/-2	500mA	5.5	0.075	80	54µA	Adj. (0.4 to 3.6)/1.2	2 x 2 DFN-6
LT3080**	1.1A***	36 (40 Abs Max)	0.3+	40	1mA	Adj. (0 to 36)++	3 x 3 DFN-8, MSOP-8E, TO-220, SOT-223
LT1965	1.1A	20	0.29	40	500µA	Adj. (1.20 to 19.5)	3 x 3 DFN-8, MSOP-8E, TO-220, DDPak
LT1963/A	1.5A	20	0.34	40	1mA	Adj. (1.21 to 20), Fixed	DDPak, TO-220, SOT-223, SO-8
LT1764/A	3A	20	0.34	40	1mA	Adj. (1.21 to 20), Fixed	DDPak, TO-220

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READERS SOLVE DESIGN PROBLEMS

Precision voltage-controlled current sink tests power supplies

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

To discover potential power-supply problems, you must run dynamic and static tests. This simple current sink tests low- to medium-power supplies and voltage sources. In this application, the current sink can draw current of 0 to 1.5A for an input-voltage range of 0 to 5V with a supply voltage as high as 20V. The basis of the circuit is precision op-amp IC_1, an OPA277 from Texas Instruments (www.ti.com), which features a maximum input-offset voltage of only 100 µV, maximum input-bias current of 4 nA, and low drift over the temperature range of −40 to +85°C (**Figure 1**). The op-amp IC compares its positive input voltage with the voltage across sense resistor R_{SENSE}.

IC_1's output drives an enhancement-mode N-channel power-MOSFET, Q_1, an STMicroelectronics (www.st.com) IRF530, such that the voltage across the sense resistor equals the positive-input voltage. The voltage across the sense resistor is proportional to the load current from the power supply under test and is independent of its output voltage. Q_1 features a maximum current of 14A at a case temperature of 25°C with drain-to-source voltage of 100V, low gate charge, and maximum on-resistance of 0.16Ω at a gate-to-source voltage of 10V and a drain current of 7A.

The MOSFET can dissipate a finite amount of maximum power—to 30W with the heat sink's thermal resistance of 1°C/W or less and an ambient temperature of 40°C or less in still air. The maximum power depends on the thermal resistance of the heat sink you use and the ambient temperature, so, when you increase the supply voltage, you must accordingly reduce the load current. By pulsing the input voltage, you can increase the supply voltage to several 10s of volts because the average power dissipation is lower and depends on the average load.

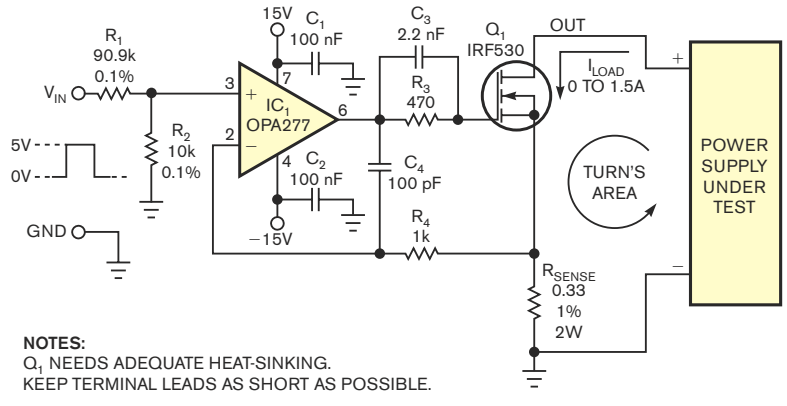

Figure 1 This simple current sink allows you to test both the static and the dynamic behavior of power supplies.

The precision resistive divider, R_1 and R_2, allows you to convert the input-voltage range of 0 to 5V into 0 to 0.495V at the positive input of IC_1, resulting in an output-current range of 0 to 1.5A. In addition, the values of resistors R_1 and R_2 provide 100 kΩ of input resistance, which is adequate for most voltage-function generators having a source impedance of 50 or 75Ω, allowing them to drive the circuit's input without using an input-op-amp buffer.

Analyzing the circuit yields the following relationships: $I_{LOAD}=GV_{IN}$, with $G=1/(\alpha R_{SENSE})=0.3A/V$, where G is the conductance, α is the attenuation factor, and $\alpha=1+R_1/R_2=10.09$. You can change the attenuation factor of the input-voltage divider to adjust

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the upper limit of the output current to several amperes, which allow you to test low-voltage power supplies with high output current.

Capacitors C_3 and C_4 and resistors R_3 and R_4 ensure loop stability, yielding a circuit with a rise time of 1.4 µsec for an input step voltage of 0 to 5V. So, you can test power supplies in either static conditions, applying a dc input voltage, or dynamic conditions, applying, for example, a pulsed input voltage to simulate fast load transients. Also, you can test power supplies or voltage sources as low as 1V because of the low channel resistance of Q_1 and the R_{SENSE} resistor; the lower limit is $1.5A(R_{SENSE}+R_{DS(ON)})=735$ mV, where $R_{DS(ON)}$ is the on-resistance.

You can also test multiple regulated outputs of power supplies such as a −5 or a −12V supply voltage. In this case, you must connect the ground of the power supply to the output of the current sink—that is, the drain terminal—and the negative output with the ground of the circuit. For accuracy, when you perform dynamic tests, such as load regulation, recovery time, and transient response, you must take care when connecting the power supply under test with the circuit to reduce the turn's area. The pulsed load current produces radiated emissions, which are proportional to this area, to the value of the current, and to the square of the current frequency, and they may disturb the circuit itself and the measuring equipment. EDN

Red LEDs function as light sensors

Geoff Nicholls, Glinde, Germany

Ordinary red LEDs normally function as light emitters, but they can also function as photosensors. A single LED can even function as both a light emitter and a light detector in the same circuit (**Reference 1**). The basic idea is to pulse the LED, using the on-time to light it and the off-time to sense the photovoltaic current from the ambient light that the LED sees.

Figure 1's circuit functions as a night-light. The LED stays off during daylight and turns on when the ambient-light level drops. The 7555 CMOS timer is a monostable one-shot, which triggers when Pin 2's voltage is less than one-third of the supply voltage. R_1 and R_2 form a voltage divider, which keeps the cathode of the LED just below the trigger voltage. When the ambient-light level is sufficient, the LED develops several hundred millivolts, which add to the R_1/R_2-junction voltage and keep Pin 2 above the one-third-trigger level. In this state, the Pin 3 output of the 7555 approaches 0V, and the 1N914 diode becomes reverse-biased, allowing the LED's photovoltaic current to flow into Pin 2's trigger input.

When the ambient-light level drops low enough, the LED voltage falls, and Pin 2 goes below the trigger level. The 7555 then generates a one-shot pulse, the 1N914 becomes forward-biased, and the LED lights up. At the end of the timing period, which R_3 and C_1 set, the monostable resets and discharges C_1. The monostable is then ready for another cycle. The LED then briefly turns off during this interval, which allows it to again sense the ambient light.

The circuit in **Figure 2** functions as a day-light; the LED flashes in bright light and stays off in low ambient light. The 7555 provides astable operation and slowly flashes the LED through the 1N914 diode as long as Pin 4's reset input is greater than approximately 600 mV. If the ambient light is too low, the LED cannot generate enough voltage at Pin 4, and the 7555 output remains near 0V, preventing the LED from turning on. The LED operates as a light emitter when Pin 3's output is high and as a sensor when Pin 3's out-

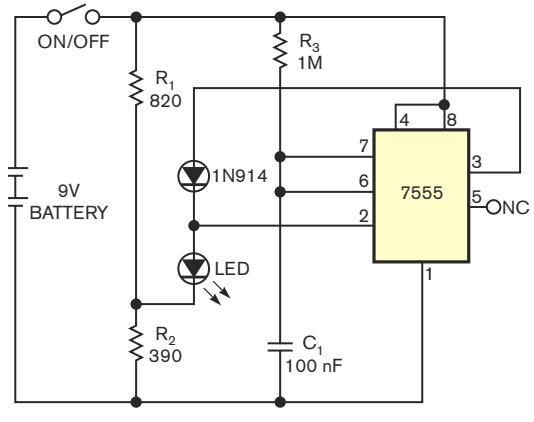


Figure 1 This circuit functions as a night-light. The LED stays off during daylight and turns on when the ambient light level drops.

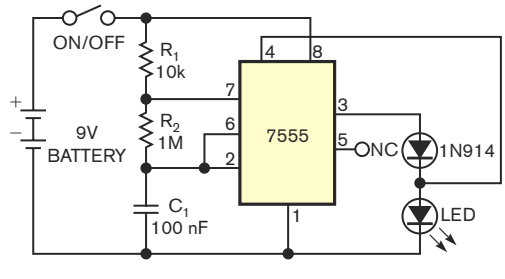
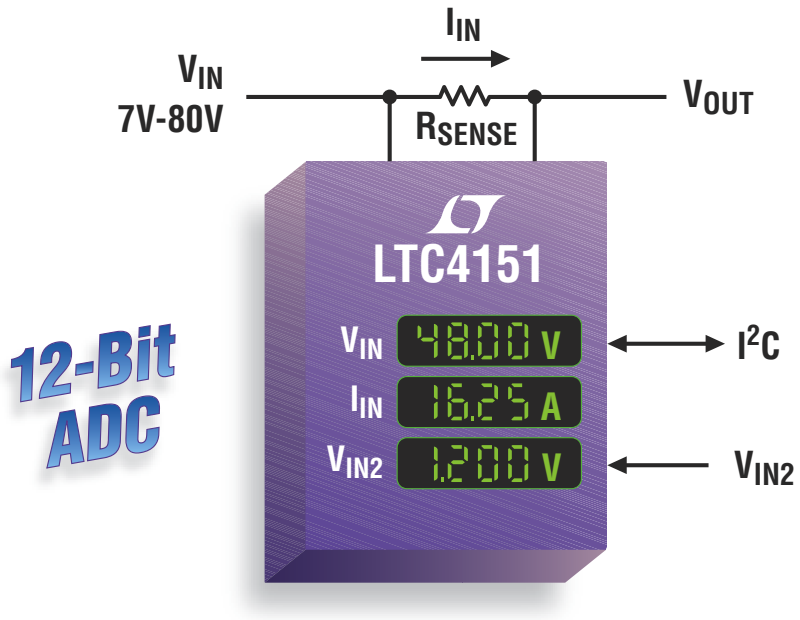


Figure 2 The LED in this circuit flashes slowly when the ambient-light level is high and turns off when the light level drops.

Measure High Voltage Power



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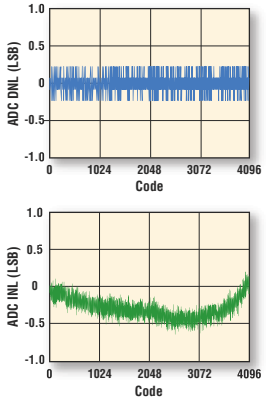

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put is low.

These circuits require no current-limiting resistor. The timer IC must be a CMOS type because, to operate correctly, the circuit design requires low input currents. The prototypes use Intersil's (www.intersil.com) ICM7555 devices.EDN

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White-noise generator has no flicker-noise component

Alfredo Saab and Randall White,
Maxim Integrated Products, Sunnyvale, CA

White-noise generators generate a flat graph of output-power density versus frequency. These generators are useful for testing circuits that have an extended low-frequency or dc response. However, the presence of pink, or flicker, noise complicates the design of white-noise generators for frequency ranges that extend to a few hertz or below. A semiconductor device generates noise that always has the characteristic signature of pink noise: Its output-power-density amplitude increases as frequency decreases, with a corner frequency of 10s of hertz to a few kilohertz. A high-value resistor generates noise with its own flicker-noise component, whose value and characteristics vary with the resistor's technology. If, on the other hand, the resistor has a low value and the device uses low-noise technology, then the noise is almost completely white with power density that is constant with frequency. Unfortunately, a low-value resistor also yields a low value of noise-power-density amplitude, and any device you introduce to amplify that level adds pink noise of its own.

You can find amplifiers whose input-voltage noise includes no pink-noise component, but their input-current noise has a flicker-noise component, which appears at the amplifier output if the resistance that any amplifier input encounters has a significant value.

In the noise-generator circuit of **Figure 1**, IC_1, a MAX4238 amplifier from Maxim (www.maxim-ic.com) has no flicker-noise component in its input-voltage noise. It amplifies its own input-voltage noise with a feedback network comprising low-value resistors to avoid adding noticeable flicker-component noise from either the resistors or the amplifier's input-noise current.

A plot of the circuit's output voltage as a function of frequency is almost flat from 0.01 Hz to 3 kHz (**Figure 2**). The voltage-density amplitude is 4 to 5 $\mu V/\sqrt{Hz}$. The noise-density amplitude also depends on temperature, so you should keep the circuit at constant temperature while making measurements.EDN

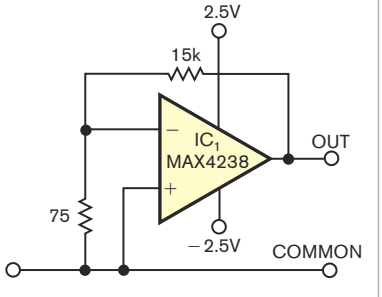

Figure 1 Built with an amplifier whose input voltage noise has no flicker-noise component, this white-noise generator produces an output with no flicker-noise component.

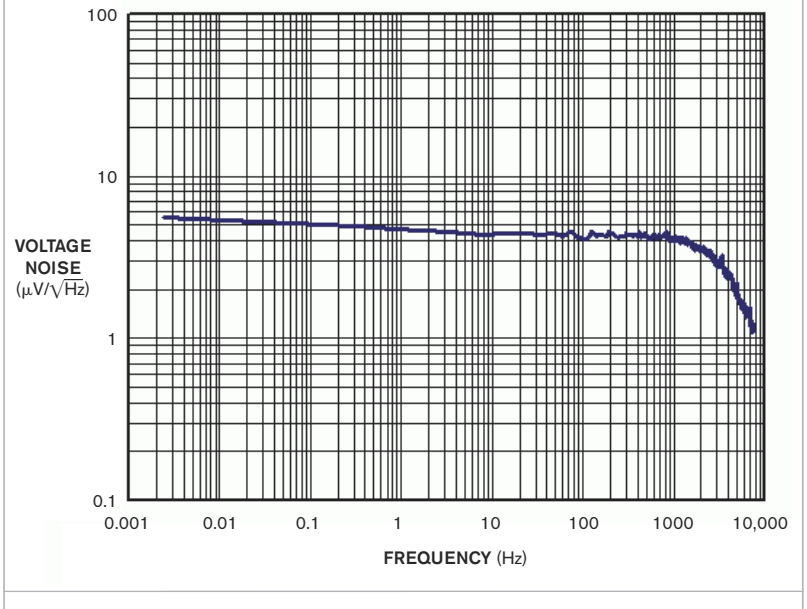

Figure 2 The circuit's output voltage as a function of frequency is almost flat from 0.01 Hz to 3 kHz.

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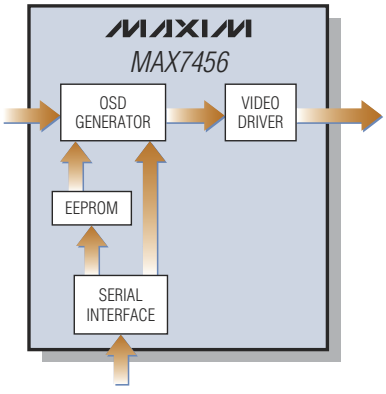

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Analog voltage controls digital potentiometer

Hrishikesh Shinde, Maxim Integrated Products, Dallas, TX

This Design Idea describes an analog voltage that controls a digital potentiometer through the device's I²C interface. An ADC in the Microchip (www.microchip.com) PIC12F683 microcontroller converts the analog voltage to the I²C stream that controls the Maxim (www.maxim-ic.com) DS1803 digital potentiometer (**Reference 1**). Of the microcontroller's six general-purpose I/O pins, two control the SDA (system-data) and SCL (system-clock-line) output signals, one controls an LED, and one accepts the analog input. SDA and SCL connect directly to the digital potentiometer's SDA and SCL pins with 4.7-kΩ pull-up resistors to V_{DD}. By adding or removing jumpers, you can separate the shared V_C and V_{DD} and isolate SDA and SCL.

The firmware is in assembly language, which was assembled using Version 7.40 of the MPLab IDE (integrated development environment), which is currently available free from Microchip at www.maxim-ic.com/tools/other/appnotes/4051/AN4051.zip. The program comprises fewer than 450 bytes in flash memory and 8 bytes in RAM. The program first initializes various configuration bits in the PIC, including the ADC and the internal oscillator. It configures the ADC to accept input from the analog input and sets the conversion clock to use the internal oscillator at 125 kHz.

The firmware runs in a loop, causing the 10-bit ADC to continuously convert the analog-input voltage. When a conversion is complete, the 8 MSBs form a data byte that transmists over the I²C bus, and this I²C-signal stream controls the digital potentiometer. The program controls both potentiometers in this dual device. With a change in firmware, however, you can independently control the potentiometers, using separate analog inputs on the PIC12F683. The program enables you to control the potentiometer by varying a voltage at the GP1 input of the PIC12F683. A change at GP1 causes a corresponding change in the potentiometer's resistance: $R_{OUT}=((\text{Input Voltage})/V_{CC})\times 50\ k\Omega$, where the end-to-end resistance of the digital potentiometer is 50 kΩ, the allowable V_{CC} range is 2.7 to 5V, and the input-voltage range is 0 to V_{CC}. You can troubleshoot an application by checking that the device's address is correct and that the I²C bus is connected. The LED blinks constantly while the ADC is running, but remains on when an I²C error occurs. After you correct the error, the LED resumes its normal function.

You can extend this design approach to other applications for which an analog voltage must control a device with an I²C interface. You can, for example, implement a nonlinear-transfer function, such as gamma correction, using the DS3906 variable resistor, and implement the transfer function in embedded look-up tables (**Reference 2**). Or, by connecting a thermistor at the input, you can vary the output of an I²C-controlled current DAC in response to changes in the ambient temperature. EDN

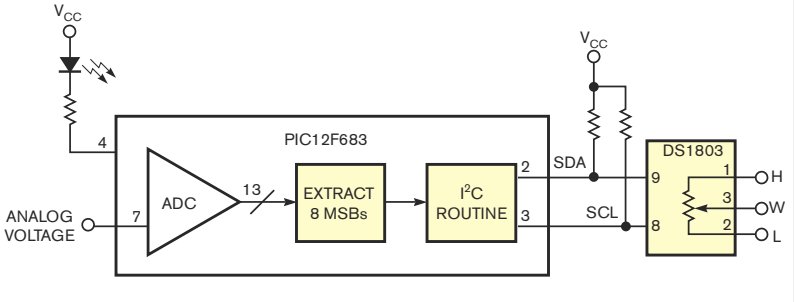

Figure 1 This circuit allows an analog-voltage input to select the digital potentiometer's resistance.

REFERENCES

1 "DS1803 Addressable Dual Digital Potentiometer," Maxim, July 25, 2007, www.maxim-ic.com/quick_view2.cfm/qv_pk/2779.
2 "DS3906 Triple NV Low Step Size Variable Resistor Plus Memory," Maxim, Aug 9, 2007, www.maxim-ic.com/quick_view2.cfm/qv_pk/4724.

Harvest energy using a piezoelectric buzzer

Carlos Cossio, Santander, Spain

Energy-harvesting, or "scavenging," systems extract energy from the ambient environment. Unfortunately, these power generators supply much less energy than do standard batteries. However, thanks to the decreasing size and low-power requirements of today's wearable devices, it is feasible to replace batteries in some low-power systems with power generators that capture energy from the user's environment, such as the vibration energy a user produces during walking or running. This Design Idea uses the piezoelectric effect of a standard and easy-to-find piezoelectric buzzer to turn mechanical vibrations into electrical energy. Although piezoelectric buzzers generate sound waves when you apply an ac voltage,

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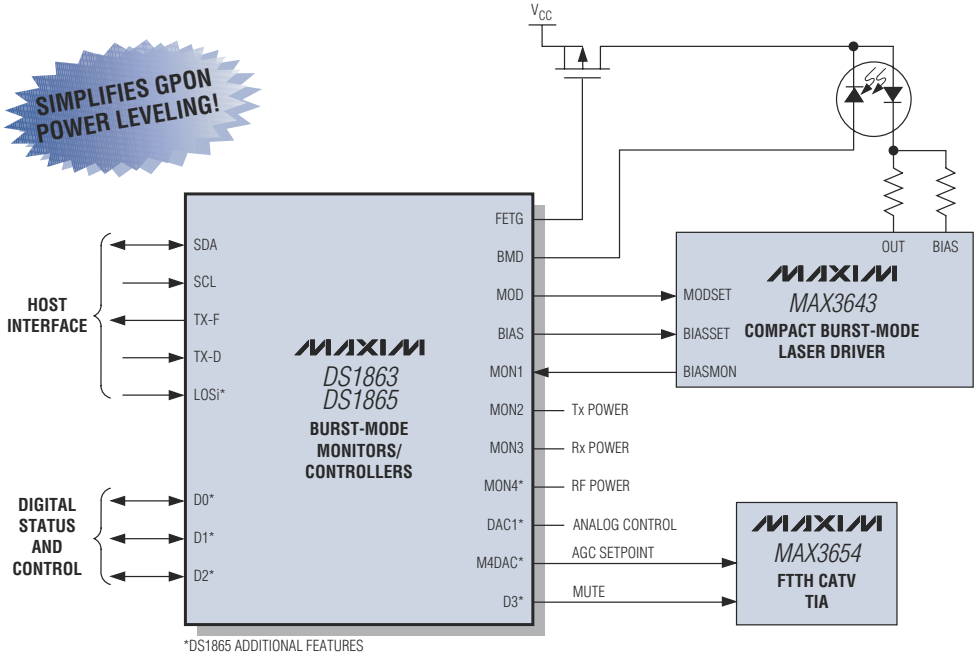

*DS1865 ADDITIONAL FEATURES

Feature	DS1863	DS1865
ADC Channels, Total (Internal)	5 (Temp, V_{CC})	6 (Temp, V_{CC})
DAC Channels, Total (Internal)	3 (APC Set)	5 (APC Set)
Laser Bias APC	✓	✓
Laser Modulation Current Temperature-Indexed Lookup Table (LUT)	✓	✓
Diplexer/Triplexer	Diplexer	Diplexer/Triplexer
I^2C Host Interface	✓	✓
Eye Safety	✓	✓
No. of GPIO and LOS Inputs	—	5
User EEPROM (Bytes)	128	256
Package	16-TSSOP	28-TQFN

MAXIM

www.maxim-ic.com/DS1863/65-info

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you can use them in the opposite way: You obtain the maximum ac peak voltage that the piezoelectric buzzer generates when the vibration frequency matches the resonant frequency of the piezoelectric buzzer.

The power generator in **Figure 1** is a simple circuit. The piezoelectric buzzer produces an ac voltage when it is under vibration; therefore, you must convert this voltage to a dc voltage before charging the capacitor. The four Schottky diodes form a bridge rectifier to perform this task. For a reliable and efficient operation, select Schottky diodes, such as the 1N5820 rectifier diode from On Semiconductor (www.onsemi.com), that exhibit low forward-voltage drop and low reverse leakage.

Energy harvesters typically capture small amounts of energy over long periods, so harvesters usually contain an energy-storage subsystem in the form of a supercapacitor, such as the PowerStor 0.47F, 2.5V capacitor from Cooper Busmann (www.bussmann.com). The larger the capacitor, the longer it takes to charge it. On the other hand, a larger capacitor provides power for a longer time for the same load. Because a supercapacitor often has a much lower voltage than standard electrolytic capacitors, you must connect a zener diode, such as the BZX85-C2V7, to prevent the voltage across the supercapacitor from increasing beyond its maximum voltage rating. As soon as you apply a load, the supercapacitor starts discharging, and the voltage across the supercapacitor starts dropping. To guarantee a fixed voltage at the output, you must use a dc/dc-voltage-converter IC, such as the MAX1675 from Maxim (www.maxim-ic.com) as a step-up converter working at 3.3V.

As an additional benefit, if the supercapacitor's voltage drops below the required voltage of operation, the circuit continues to provide regulated output voltage as long as the supercapacitor voltage does not drop below the lower limit of the dc/dc converter. This limit is 0.7V for the MAX1675. EDN

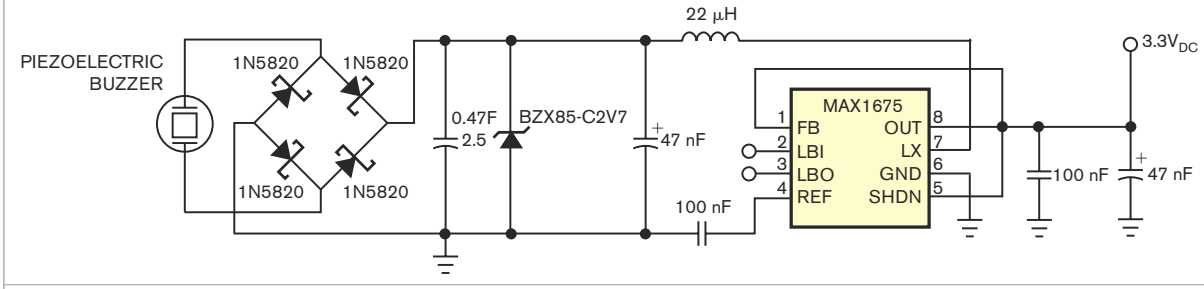

Figure 1 A simple vibrational-energy-harvesting circuit using an off-the-shelf piezoelectric buzzer as the power generator turns mechanical energy into electrical energy.

Retriggerable monostable multivibrator quickly discharges power-supply capacitor

Jordan Dimitrov, Tradeport Electronics, Vaughan, ON, Canada

Universal power supplies must work from mains power lines ranging from 90 to 264V ac at 50 or 60 Hz. Directly rectifying the input voltage charges the filter capacitor to 120 to 370V dc. Such voltages present a serious threat to personnel who are prototyping or repairing the power supply. It is desirable to discharge the filter capacitor when mains power is off so workers can safely deal with the power supply. An intuitive solution is to use an ac relay. However, relays cannot operate in a wide range of input voltages, they consume significant power and space, and they have a limited number of cycles. **Figure 1** shows an alternative circuit, which you can apply to a filter capacitor of almost any value. It uses a MOSFET, Q_1, and a current-limiting resistor, R_D, to discharge the high-voltage filter capacitor, C_F, within one second after you switch off the mains power. The trick is to use a retriggerable monostable multivibrator to control the MOSFET.

THE TRICK IS TO USE A RETRIGGERABLE MONOSTABLE MULTIVIBRATOR TO CONTROL THE MOSFET.

While the mains power is on, optocoupler IC_1 and the associated passive components continue to generate symmetrical square pulses that they apply to the A input of multivibrator IC_2. Each pulse triggers the circuit, forcing the $\overline{Q}$ output to the low level. The multivibrator generates a 100-msec negative pulse; then, $\overline{Q}$ should turn high. However, because triggering pulses arrive before the multivibrator's pulse is complete, the $\overline{Q}$ output never turns high, the MOSFET is always off, and the rectifier works as usual. When you turn off mains power, the $\overline{Q}$ output stays low for 100 msec after the last triggering pulse;

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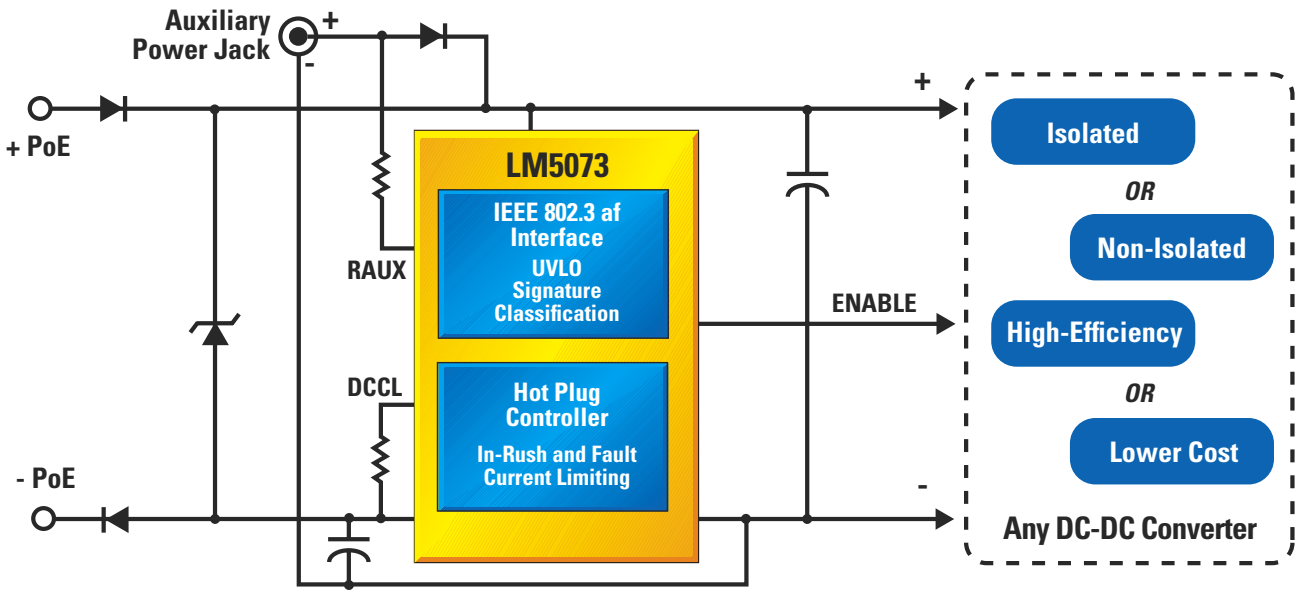

Product ID	Abs Max V_{IN} (V)	Hot Swap FET Rds(on) Typ (Ω)	DC Operating Current Limit	Auxiliary Power Support[1]	Integrated DC-DC Converter	Packaging
LM5070	76	1	Fixed 390 mA	Front only	✔	TSSOP-16
LM5071	76	1	Fixed 390 mA	Front or rear	✔	TSSOP-16
LM5072	100	0.7	Programmable to 800 mA	Front or rear, dominant or non-dominant	✔	TSSOP-16EP
LM5073	100	0.7	Programmable to 800 mA	Front or rear, dominant or non-dominant	—[2]	TSSOP-14EP

[1] Front auxiliary power is coupled though the PD interface. Rear auxiliary power is coupled to the input of the DC-DC converter. Dominant auxiliary power supersedes PSE power when the auxiliary source is connected.
[2] Operates with a wide range of isolated or non-isolated DC-DC solutions

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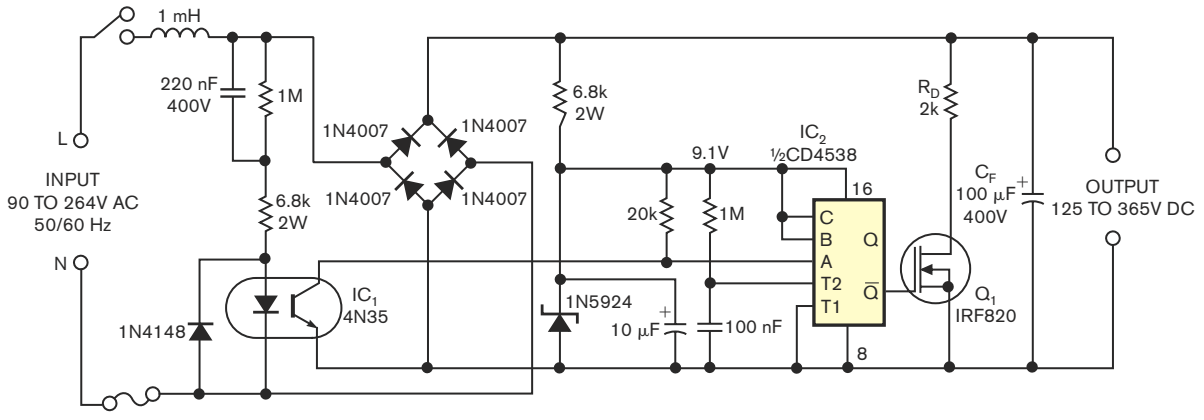

Figure 1 Because of the retriggerable feature of the CD4538 IC, the discharge network, Q_1 and R_D, remains off when mains power is present; otherwise, it turns on and quickly discharges high-voltage filter capacitor, C_F.

it then turns high. The MOSFET turns on and quickly discharges the output capacitor to a safe level.

The circuit underwent testing at both limits of the input voltage: 90 and 264V ac. The filter capacitor is of moderate value, 100 µF, and so is the peak-discharge current of 0.06 to 0.18A. The MOSFET's peak current is 8A; hence, the circuit can readily work with much larger-value capacitors. If this current is still not enough, you must use a MOSFET with a higher peak current rate. You need to change only R_D to fit the desired discharge time, t_D. The $t_D=3\times R_D\times C_F$ relationship is a good guideline. It ensures that the output voltage drops to 95% of its initial value, which is well below the user-touchable safety limit for any value of the output voltage. EDN

LINEAR TECHNOLOGY

DESIGN NOTES

Hot Swap Solution Meets AMC and MicroTCA Standards

Design Note 437

Vladimir Ostrerov

Introduction

The LTC®4223 is a dual Hot Swap™ controller that meets the power requirements of the Micro Telecommunication Computing Architecture (MicroTCA) specification recently ratified by the PCI Industrial Computer Manufacturers Group (PICMG).

The LTC4223 includes an internal pass FET for the 3.3V auxiliary supply and a driver for an external N-channel pass FET for the 12V payload supply. Inrush current for both supplies is controlled: the auxiliary supply has a fixed 240mA active current limit and the 12V ramp rate is controlled by an external capacitor. A timed circuit breaker and fast current limit protect both supplies against severe overcurrent faults. It also features an adjustable analog current limit with a circuit breaker timeout for the 12V supply.

The LTC4223 monitors 12V load current by sensing voltage across an external resistor and outputs a ground-referenced voltage (at the 12IMON pin) proportional to the load current. It also provides separate power-good outputs for the two supplies and a single, common fault output. Additional features include card detection and independent control of the two supplies. The LTC4223-1 latches off after a circuit breaker fault timeout expires while the LTC4223-2 provides automatic retry after a fault. A fault on the 12V supply shuts down only the 12V path, leaving the 3.3V auxiliary power available for system management functions. A fault on the 3.3V AUX supply shuts down both supplies.

Advanced Mezzanine Card Application

Figure 1 shows a typical MicroTCA application. The current limit on the 12V rail is 7.6A, determined by the 6mΩ

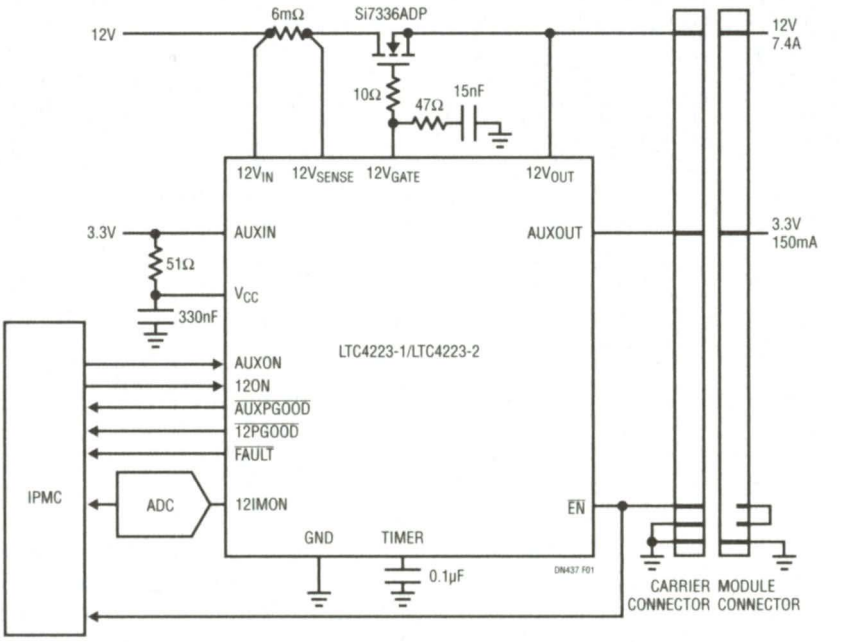

Figure 1. Advanced Mezzanine Card Application

sense resistor. Auxiliary rail current limit is internally set to 240mA. (Section 4.2.1 of the MicroTCA specification details the requirements for payload and auxiliary voltage, current, and protection.) Figure 2 shows the power-up transients when a card is inserted. Figures 3 and 4 show the two modes of overcurrent protection on the 12V supply. In Figure 3, the load current is increased above the analog current limit (ACL) threshold. The LTC4223 responds by reducing the current to the ACL threshold, allowing the card to ride out short overcurrent faults. If the fault persists, the timer expires and power is turned off. In the event of a severe overcurrent fault, load current is reduced to the ACL limit in 8µs as shown in Figure 4. Once again, if the fault persists and the timer expires, power is turned off entirely.

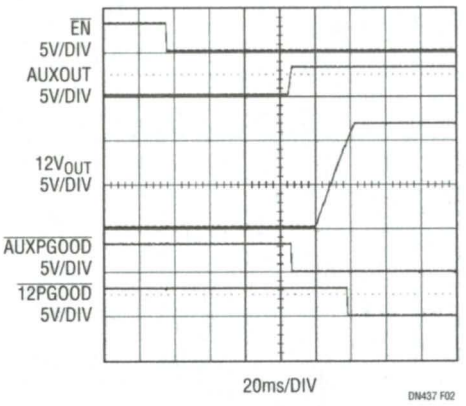

Figure 2. Normal Power-Up Waveform

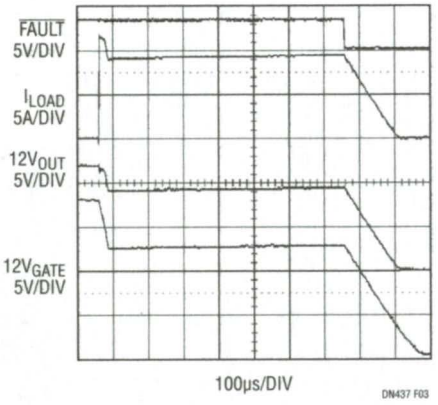

Figure 3. Overcurrent Fault on 12V Output

Conclusion

The LTC4223 aims to simplify Hot Swap control for Advanced Mezzanine Cards in ATCA and MicroTCA systems. It succeeds by meeting all MicroTCA requirements for controlling both payload and auxiliary power with only a 5mm × 4mm DFN package and a few minimal external components. Individual card monitoring and control functions are further simplified by LTC4223's status and control lines.

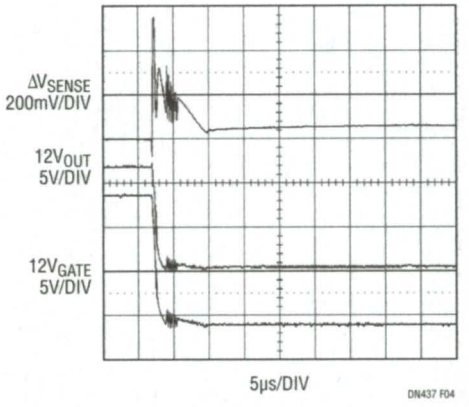

Figure 4. Short-Circuit Fault on 12V Output

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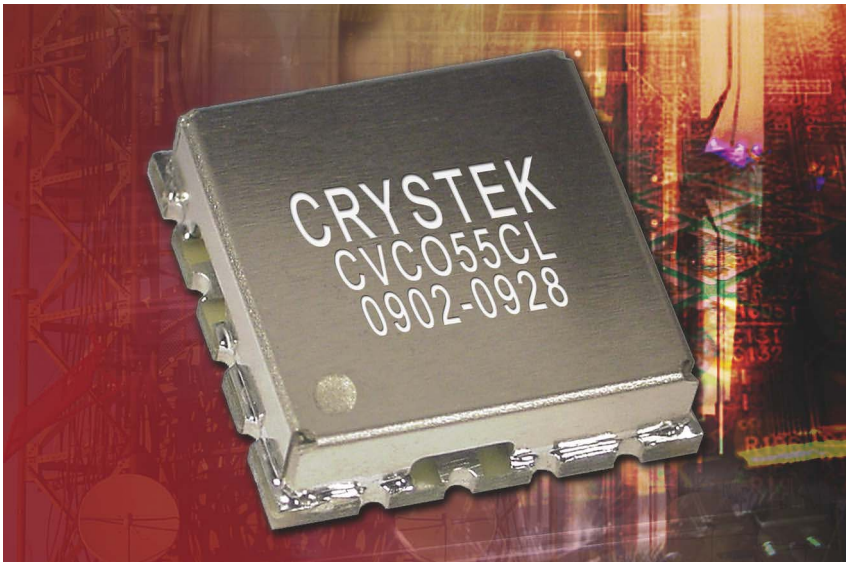

VCO operates from 902 to 928 MHz

The CVCO55CL VCO (voltage-controlled oscillator) operates at 902 to 928 MHz and has a 0.5 to 4.5V control-voltage range. Features include 5V input voltage, 20-mA current consumption, −115 dBc/Hz at 10-kHz offset, and −15-dBc typical second-harmonic suppression. The device also provides pushing and pulling at 2 MHz and 0.8 MHz/V, respectively. Available in a 0.5×0.5-in. SMD package, the CVCO55CL VCO costs $9.11.

Crystek Corp, www.crystek.com

Precision-power op amp aims at high-voltage applications

Suiting optical communications, industrial control, data acquisition, and power supplies and regulators, the unity-gain-stable OPA454 precision-power op amp operates on 100V supplies and provides ±50-mA output currents with a 150-mA short-circuit limit. The amplifier includes a 10V/μsec and a 2.5-MHz gain bandwidth, a ±4V (8V)±50V (100V) single or dual supply, a ±110-pA bias current, a 4-mV maximum-dc-accuracy offset, and 5-μV/°C drift. An output-status flag referenced to the common pin tells the user when an overcurrent or thermal-overload condition occurs. PowerPad technology includes an exposed metal pad allowing heat sinking over the −40 to +125°C industrial-operating-temperature range. Additional features include a fast-acting enable/disable pin referenced to the common pin, which can be ground. Available in an SO-8 PowerPad package, the OPA454 op amp costs $3.45(100).

Texas Instruments, www.ti.com

Active-bypass power-amplifiers claim an improved low-power efficiency

Based on the fifth generation of the vendor's CoolPAM technology, the ACPM-7353 active-bypass power-amplifier family supports high-, mid-, and active-bypass power modes. The am-

AMPLIFIERS, OSCILLATORS, AND MIXERS

plifier supports dual-band frequencies and offers a simplified power-amplifier design with an RF input port for each band. The devices lower the average current of the CDMA transmitter usage, conserving power consumption. Claiming a 10% increase in battery life compared with previous generations, the amplifiers provide a 3-mA quiescent-current level, with 10-dB gain and 11-dBm output-power levels. Measuring 4×5-mm, the ACPM-7353 costs $1.90 (1000).

Avago Technologies, www.avagotech.com

Voltage-feedback amplifier reduces input noise

Targeting densely populated, thermally sensitive instrumentation equipment requiring high-speed signal conditioning, the ADA4857 high-speed op amp consumes 5 mA and operates at 850 MHz. The voltage-feedback amp provides 4.4-nV/$\sqrt{Hz}$ input noise and −91-dBc distortion at 10 MHz. Measuring 3×3 mm, the single-channel ADA4857-1 amplifier comes in eight-lead LFCSPs (lead-frame chip-scale packages) and eight-lead SOIC (small-outline-IC) packages; the dual ADA4857-2 comes in 4×4-mm, 16-lead LFCSPs. The ADA4857-1 and ADA4857-2 cost 85 cents and $1.39 (1000), respectively.

Analog Devices, www.analog.com

Audio-line driver suits television peripherals

The DRV601 DirectPath audio-line driver targets set-top boxes, HDTV receivers, DVD players, gaming consoles, and portable media players. The device provides a 2V-rms/channel output voltage into 600Ω at 3.3V. The 4×4-mm, QFN package integrates a charge pump, allowing an audio-output signal chain to operate from a 3.3V power supply. Features include a 1.8 to 4.5V power-supply range, an independent right- and left-channel shutdown control, short-circuit and thermal protection, and pop-reduction circuitry. The driver also provides a dynamic range greater than 105 dB. The DVR601 costs 90 cents (100).

Texas Instruments, www.ti.com

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COMPUTERS AND PERIPHERALS

Solid-state drives use the vendor's eight-channel ASIC controller

The Mach8-IOPS (input-output/sec) solid-state drive uses the vendor's proprietary eight-channel ASIC controller, making the device suitable for enterprise-class hard-disk drives. The drives deliver more than 10,000 random-read IOPS and more than 1000 random write IOPS. They also provide 100-Mbps sustained sequential performance for reads and writes. The Mach8-IOPS is available in 8-, 16-, 32-, 64-, 128-, and 256-Gbyte versions and sells for $12 to $15 per gigabyte.

Stec, www.stec-inc.com

Graphics card provides a 100% h.264 video-decoding offload

The 512-Mbyte XLR8 GeForce 8800 GTS (gigatexel shader) PCIe (PCI Express) 2.0 graphics card claims a 100% offload of H.264 video decoding from the processor. Features include 128 stream processors clocking at 1.625 GHz; a 256-bit, 512-Mbyte frame buffer running at 1940 MHz; and a 5-GT (gigatexel)/sec PCIe 2.0 bandwidth. The devices also provide analog standard-definition-TV/high-definition-TV output, two dual-link DVI (digital-visual-interface) connectors, and integrated dual-link HDCP (high-definition-copy-protocol) support. The XLR GeForce 8800 supports Nvidia SLI (scalable-link-interface) technology and costs $359.99 to $409.99.

PNY Technologies, www.pny.com

Optical-disc drive features real-time recording

The TruDirect SE-S204S optical-disc drive allows real-time recording from most digital devices. Features include 20× DVD+R and DVD−R writing, 16× DVD+R dual-layer writing, 12× DVD−R dual-layer writing, and 12× DVD−RAM writing. The TruDirect SE-S204S optical-disc drive costs $159.99.

Samsung Electronics, www.samsung.com

Mini-PCIe card allows 802.11n wireless connectivity

The Aria Extreme-n 802.11n wireless mini-PCIe (PCI Express) card provides 802.11n wireless-network connectivity to Mac Pro, MacBook, MacBook Pro, Intel-based iMac, Intel-based Mac mini, and Windows notebook computers with an available mini-PCIe slot. The device is backward-compatible with 802.11a, 802.11b, and 802.11g devices. Measuring 2×1.125-in., the Aria Extreme-n card costs $129.95

Sonnet Technologies, www.sonnettech.com

Optical drive receives an external redesign

With a new exterior for the vendor's EZ-Dub optical drive, the DX-20A4PU model provides touch-sensitive buttons on top of the unit, as well as a rear power switch. The rewritable DVD Dual± format drive provides 8.5 Gbytes in double-layer capacity. The device also provides a 20× DVD write speed. The DX-20A4PU EZ-Dub optical drive costs $99.

Philips & Lite-On Digital Solutions, www.pldsnet.com

65-in. LCD TV provides a 2000-to-1 contrast ratio

Suiting commercial applications, the 65-in. MultiSync LCD6520


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COMPUTERS AND PERIPHERALS

LCD TV provides a 1920×1080-pixel, high-definition resolution with a 2000-to-1 contrast ratio. Additional features include a 6-msec response time, Ambix+T Technology supporting digital and analog inputs, the vendor's Digital Signage Technology suite, and an optional digital tuner available for a landscape model. The LCD6520L-AV and LCD6520P-AV cost $18,499.99 and $19,999.99, respectively.

NEC Display Solutions, www.necdisplay.com

SSD devices come in 19 options

The vendor's 19 new SSDs (solid-state drives) devices include 1.8-, 2.5-, and 3.5-in.-form-factor SATA (serial-advanced-technology-attachment) devices and 1.8- and 2.5-in. IDE PATA (parallel-advanced-technology-attachment) devices. Interchangeable with traditional hard drives, the SSDs provide significant increases in shock and vibration resistance. Operating over a −40 to +85°C industrial-temperature range, the 2.5-in. SS28A5C25I costs $4000.

Super Talent Technology, www.supertalent.com

Encrypted, portable hard drive has password protection

The Aegis Vault secure portable-storage system features 128-bit AES (Advanced Encryption Standard) hardware with password protection. The 2.5-in., bus-powered drive provides robust, 16-point, omnidirectional shock mounting and the vendor's integrated USB cable. Available in 80-, 120-, 160-, and 250-Gbyte capacities, the Aegis Vault costs $139, $169, $199, and $269, respectively.

Apricorn, www.apricorn.com

TEST AND MEASUREMENT

Digitizer/oscilloscope PCIe cards allow synchronization of 542 channels

The UF2e-2020 and UF2e-2021 8-bit digitizer/oscilloscope PCIe (PCI Express) cards feature dual-timebase sampling, synchronous digital inputs, asynchronous digital I/O, and the ability to synchronize as many as 542 channels. The UF2e-2020 provides two 50M-sample/sec rates, and the UF2e-2021 provides four 50M-sample/sec rates. Each channel has an 8-bit ADC for simultaneous sampling, seven programmable input voltages from ±50 mV to ±5V, a 400% offset adjustment, and 50Ω and 1-mΩ input impedances. The cards' 4G samples of onboard memory allows them to record signals for 40 seconds on two channels or 20 seconds on four channels. The UF2e-2020 and UF2e-2021 8-bit digitizer/oscilloscope PCIe cards cost $3190.

Strategic Test Corp, www.strategic-test.com

PCIe card has a two-channel AWG

The two-channel, 125M-sample/sec, 8-bit UF2e-6110 AWG (arbitrary-waveform-generator) PCIe (PCI Express) card features synchronous-multichannel capability. Each channel has an 8-bit DAC, allowing synchronous output and an option of three fifth- and fourth-order, lowpass-reconstruction Butterworth filters providing 500-kHz, 5-MHz, or 25-MHz bandwidth. The device also provides a software-selectable no-filter option. The UF2e-6110 PCIe cards cost $4790.

Strategic Test, www.strategic-test.com

productroundup

EMBEDDED SYSTEMS

Low-power controller features Intel Celeron M processor

Aiming at low-power embedded-system applications, the GEME-42000 PC-based controller runs continuously in critical applications, such as machine tools and digital-video capture. The controller comes with an ultralow-voltage, 1-GHz Intel Celeron M processor and as much as 1 Gbyte of DDR333 RAM. Users can control the $925 (one) GEME-42000 from remote locations.

Adlink Technology, www.adlinktech.com

CompactPCI PC series includes three single- and dual-core Intel processors

Using a high-performance and long-term supply-processing chip set from the Intel Embedded Architecture, the ITC-320 series comprises a range of 3U CompactPCI embedded-blade single-board computers. The series features three types of single- and dual-core Intel processors and four environmental architectures, including a rugged conduction-cooled version. The dual-core, 1.5-GHz Intel Core 2 dual LV processor suits signal- and data-processing applications, the 1.2-GHz Intel Core Duo processor claims a compromise between computing performance and low power consumption, and the 1-GHz Celeron M processor suits applications in which power dissipation is a critical issue. The ITC-320 series costs $2600.

Thales, www.thalescomputers.com

5.7-in. TFT display offers sunlight readability

The PDI-T320240SR-5.7 sunlight-readable 5.7-in. TFT (thin-film-transistor) modules provide a 320×240 QVGA resolution. High-intensity white LEDs provide a 300-cd/m^2 typical brightness. Additional features include a 400-to-1 contrast ratio and a 15-msec response time. The PDI-T320240SR-5.7 sunlight-readable module costs $87.25; a transmissive module and a transmissive model with touch capability are available for $62.50 and $71.85, respectively.

Phoenix Display International, www.phoenixdisplay.com

Evaluation kit provides FPGA-design capabilities for embedded systems

Combining a Cyclone III starter board and a touch-screen LCD, the Nios II embedded evaluation kit Cyclone III Edition provides an 800×480-pixel color touch-panel LCD and an SD-card interface with an SD-flash card. The kit includes the Nios II EDS (embedded-design suite) for embedded-software development, several tutorials, and design examples with full source code, easing software development for the Nios II embedded processor. Features include a 3C25 FPGA with 25,000 logic elements, 32-Mbytes of DDR SDRAM, 1 Mbyte of SSRAM, a 16-Mbyte flash memory, and a 10/100-Mbps Ethernet PHY (physical) layer. The Nios II evaluation kit costs $399.

Altera Corp, www.altera.com

General-purpose I/O card has a 400,000-gate FPGA

The general-purpose programmable 5I23 industrial I/O card aims at PCI buses. Claiming to be an Anything I/O card, the device uses a 400,000-gate Xilinx FPGA for logic. A downloadable FPGA configuration from the PCI-bus side allows creation of most specialized I/O functions. The 5I23 I/O card costs $153 (100).

Mesa Electronics, www.mesanet.com

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BY PIERRE RENAUD • HARDWARE ENGINEER

The case of the bad memory chip

DANIEL VASCONCELLOS

Although this event happened years ago, its lesson still remains as one of the more important laws of the art of debugging: Bugs don't disappear with time. It all started one day when my boss called me and another co-worker into his office for an urgent task. It seems that our telephone switches were failing to perform the one crucial operation of a redundant system: to switch activity from one machine to another. The top brass directed every lab location with such a switch to investigate the problem. The only clue was that the bug began to manifest itself with the latest memory boards.

Everyone thought the culprit was a bad batch of DRAM chips because the older boards had been in the field for years, and this problem had never occurred before. So, my boss assigned me, the hardware guy, to team up with my software buddy to see if we could diagnose the problem.

Considering the number of labs and the number of people working on the case, we never thought that we would be of much use. But we headed toward the lab anyway. Our first step was to understand how a successful activity switch works by forcing one to occur with the good old memory boards installed in both halves of the system. Sure enough, the system switched correctly several times when we prompted it from the command console. Then, I replaced a memory board with one incorporating the "bad" chips on the standby side, and the switch command failed. When I asked my colleague what could cause the master to refuse to relinquish control to the standby side, he said that the master had most likely found the standby's data tables to be corrupt, thereby preventing the switch from occurring.

Scanning the memory dump, it looked as if that corruption had occurred, except that the table pointers turned out to be the culprits. Instead of reading FFFF0000, as a good card should, the pointers read FF00FF00. This alternating pattern was a telltale sign of what occurs just after DRAM data powers up. The DRAM seemed to be not initializing. At this point, my colleague assured me that the boot software had been around since the start of the product, and it had always worked. And besides, the other pointer FFFF0000 was correct because it pointed to the proper location. I suggested we manually change the pointer value on the bad card and execute the boot code.

The value remained unchanged, as if we had never initialized it. My buddy insisted it was a hardware problem.

"You must be right," I said, to prevent the usual hardware-versus-software finger-pointing match. "But let's repeat the process on the good card."

"Why?" he asked. "We can see the correct value." At this point I had a hunch, and I urged him to try it out. To his amazement, the boot code failed to correctly initialize the pointers. I then told him that both pointers were simply different patterns of alternating FF and 00 and most likely the result of different internal geometries for both types of DRAM chips. He looked through the code and found the bug that the original DRAM pattern had masked and buried for years.

When we reported our findings, our boss did not believe us and sent us back down to the lab. I can't remember our getting any kind of recognition. It was as if the bug had never occurred. Most likely, some very important person hushed up the whole affair due to the embarrassing nature of the problem. But my buddy and I never forgot how great we felt when we found that bug. EDN

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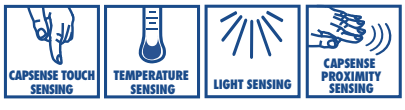

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